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CONFERENCE CATALOG

PCB WEST 2018

Conference & Exhibition

Conference:
September 11 – 13
Exhibition:
Wednesday, September 12
Santa Clara Convention Center, CA

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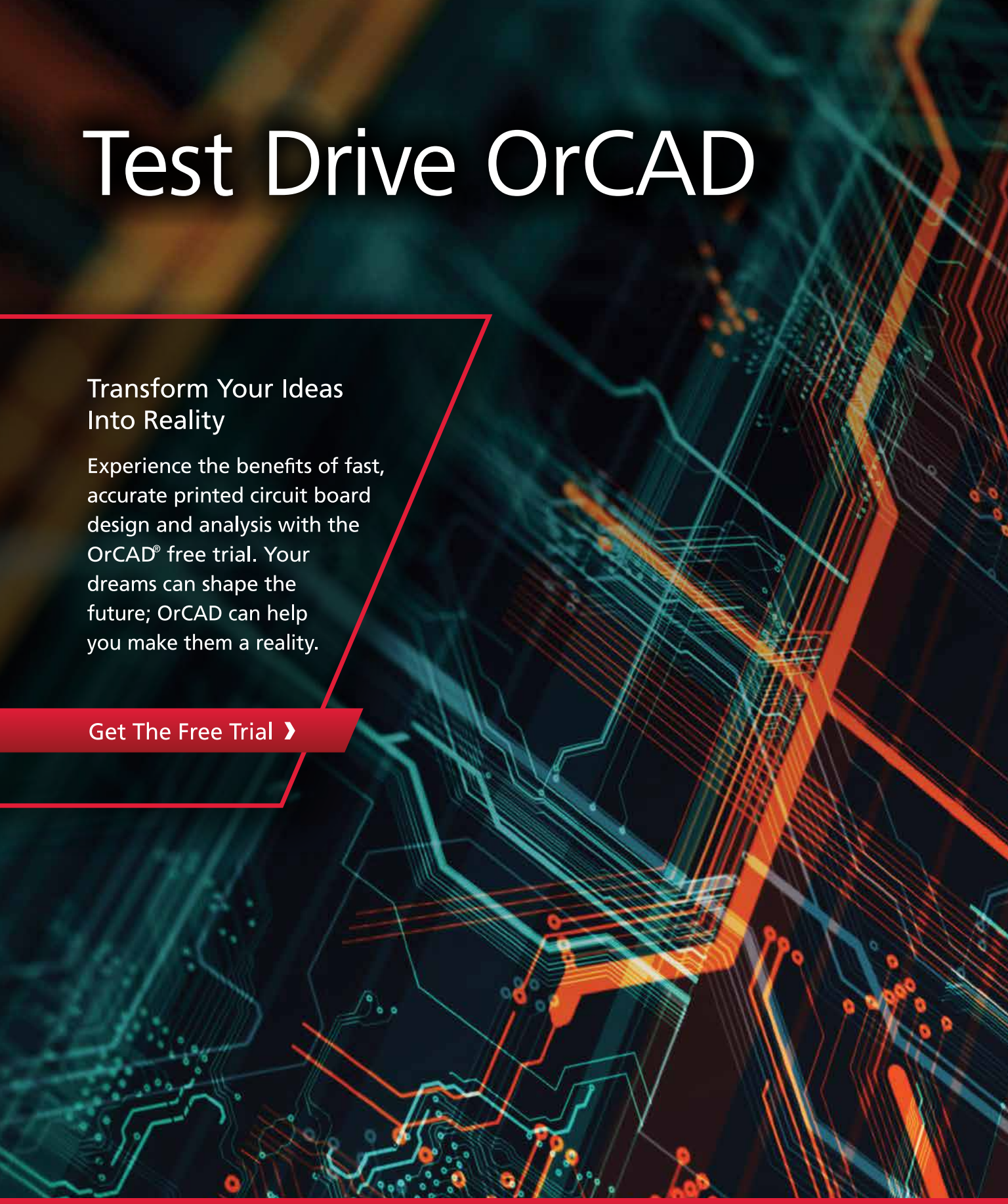
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FROM THE CONFERENCE CHAIR

For 27 years PCB West has trained designers, fabricators and, lately, assemblers on making printed circuit boards for every product or use imaginable. How far we've come! Last year's event attracted nearly 2,000 designers and engineers and more than 100 exhibitors for the three-day technical conference and sold-out exhibition.

From high reliability military/aerospace to cutting-edge IoT and wearables, there's something for everyone involved in the electronics supply chain. And we've added tracks for fabricators and assemblers as well. This is one show you cannot afford to miss. See you in September!

Mike Buetow

VENUE AND TRAVEL INFO:

EVENT LOCATION

Santa Clara Convention Center
5001 Great America Parkway
Santa Clara, CA 95054
408-748-7000
santaclara.org/conventioncenter

- Easy access from Interstate 101
- Free parking
- Attached to the Hyatt Regency Santa Clara Hotel

AIRPORTS

San Jose International Airport (SJC)
Hotel direction: 4 mi south
Estimated taxi fare to hotel: $17 (one way)
San Francisco (SFO)
Hotel direction: 30 mi south
Estimated taxi fare to hotel: $90 (one way)

SHUTTLE INFORMATION

The Santa Clara Convention Center and Hyatt Regency Santa Clara are located just 12 minutes (6 miles) from Mineta San Jose International Airport (SJC) and 35 minutes (31 miles) from San Francisco International Airport.

Super Shuttle is offering PCB West attendees a 10% discount on all services. To book a shuttle in advance, please click the below link: http://groups.supershuttle.com/pcbwest.html

HEADQUARTERS HOTEL

Hyatt Regency Santa Clara
5101 Great America Parkway
Santa Clara, California, USA, 95054

2018 Group Rate: $309/night.
Reservations can be made by calling 408-200-1234 or 888-421-1442 or https://aws.passkey.com/go/pcbwest18
Please be sure to mention "PCB West 2018" to ensure you get the blocked rate.
The deadline to reserve a room is August 20, 2018.
As the block rate sells out, any reservation made will be based on availability, and prevailing rates will apply.

CONFERENCE PRICING AND POLICIES

Register by the Early-Bird Deadline of August 13 to save up to $100

ROW SEAT

SECTION
FREE
EXHIBITION ONLY
12 SEPTEMBER 2018

Exhibition Only Pass
FREE!

(Wed., September 12 Only)

Admission to the following events on Wednesday, September 12:
One-day exhibition
FREE technical sessions
Lunch and an evening reception

ROW SEAT

SECTION
BEST VALUE
3-DAY
ALL-INCLUSIVE
TECHNICAL
CONFERENCE PASS
11-13 SEPTEMBER 2018

3-Day All-inclusive Technical Conference Pass
BEST VALUE!

$1195 through August 13 ... $1295 after August 13 (Tues., September 11 – Thurs., September 13)

3-Day technical conference pass includes:

Choice of any conference sessions during the entire Tuesday, Wednesday and Thursday technical conference
One copy of the conference proceedings
Lunch-n-Learn sponsored by Streamline Circuits on Tuesday
Lunch-n-Learn sponsored by Polar Instruments on Thursday
Conference WiFi sponsored by Mentor
Conference Coffee sponsored by Sierra Circuits
Admission to the following events on Wednesday, September 12:

- One-day exhibition
- FREE technical sessions
- Lunch break sponsored by Sierra Circuits
- Evening reception sponsored by Ultra Librarian

One-day Technical Conference Pass Options:

$595 per day through August 13...$695 per day after August 13

(Choose One Day Only: Tues., September 11; Wed., September 12; OR Thurs., September 13)

One-Day Tuesday Technical Conference Pass

Tues., September 11:

Choice of any conference sessions on Tuesday
Lunch-n-Learn sponsored by Streamline Circuits
Admission to the following events on Wed., Sept. 12th:

- One-day exhibition
- FREE technical sessions
- Lunch sponsored by Sierra Circuits
- Evening Reception sponsored by Ultra Librarian

ROW SEAT

One-Day Wednesday Technical Conference Pass

Wed., September 12:

Choice of any conference sessions on Wednesday
Admission to the following events on Wednesday, September 12th:

- One-day exhibition
- FREE technical sessions
- Lunch sponsored by Sierra Circuits
- Evening Reception sponsored by Ultra Librarian

ROW SEAT

One-Day Thursday Technical Conference Pass

Thurs., September 13:

Choice of any conference sessions on Thursday
Lunch-n-Learn sponsored by Polar Instruments
Admission to the following events on Wed., Sept 12th:

- One-day exhibition
- FREE technical sessions
- Lunch sponsored by Sierra Circuits
- Evening Reception sponsored by Ultra Librarian

ROW SEAT

Note: The conference proceedings are NOT included in the one-day pass. During registration you will have the option to add a copy for $200.

REGISTER NOW!

IPC 4-DAY DESIGNER CERTIFICATION PROGRAMS

September 7 – 10, 2018

Questions regarding the IPC Certification Program? Please contact Cheryl Fisher at 800.643.7822 x223 or cherylfisher@eptac.com.

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IPC Advanced Designer Certification Program (CID+)

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Continuing the educational series for PCB Design, the IPC Advanced Designer Certification or CID+ (Advanced Certified Interconnect Designer) is the ultimate professional industry certification for a designer looking to obtain what we would consider a master's in PCB Design.

Questions?

Contact the PCB West Registration Desk at 855.290.2441

Payment Policies:

All payments for the conference must be received prior to attending. Payments can be made by credit card, check or wire transfer. Registrations without complete payment information will not be processed.
Check payments should be made to UP Media Group, Attn: PCB West 2018, P.O. Box 470, Canton, GA 30169.
ALL wire transfers are charged a $50 processing fee per registration.
Credit card payments will show a charge from UP Media Group.

Refunds and Cancellations:

A $25 cancellation fee will be withheld from any registration fees refunded. All refund requests must be made in writing no later than August 21, 2018, Attn. Alyson Corey, acorey@upmediagroup.com. "No shows" who have not made a written request by August 21 are fully liable for conference tuition/fees. Registrations made after August 21 are considered confirmed, and no refund requests will be accepted; registrants will be fully liable for conference tuition/fees and will be invoiced accordingly.

REGISTER NOW!

TUESDAY, SEPTEMBER 11

TITLE	SPEAKER	CATEGORY
8:00am CONFERENCE COFFEE BREAK, *Sponsored by Sierra Circuits*		
8:30am - 12:00pm		
1: PCB Design Strategy for High Density BGA and CSP Components	Vern Solberg, Solberg Technical Consulting	DfF/DfM/DfA/DfT
9:00am - 11:00am		
2: Layout of Switch Mode Power Supplies	Rick Hartley, RHartley Enterprises	EMI/EMC/PCB Design
3: Power Distribution Made Easy	Daniel Beeker, NXP Semiconductor	PCB Design/Layout/ Placement
9:00am - 5:00pm		
4: The Basics of PCB Design	Susy Webb, Fairfield Industries	PCB Design/Layout/ Placement
5: What's New in the IPC Design Standards, and How to Use Them	Gary Ferrari, FTG Circuits	PCB Design/Layout/ Placement/Standards
6: PCB Stackup Design and Materials Selection	Bill Hargin, Z-zero	PCB Design
7: Troubleshooting and Defect Resolution of SMT Assembly Processes	Jim Hall and Phil Zarrow, ITM Consulting	SMT/Electronics Assembly
10:00am - 11:00pm		
25: Continuing Test Point Management throughout a PCB Design Flow	Mark Laing, Mentor	PCB Design/Layout/ Placement
11:00am - 12:00pm		
8: Managing Your Impedance, Coupling and Return Paths in Design and Avoid Unnecessary Iterations with SI/PI Engineers	Dennis Nagle, Cadence Design Systems	High Speed
9: Evaluating an Appropriate Power Plane through Power Integrity Simulation	Richard Villamor Legaspino, Analog Devices	Power Integrity
27: ECAD-MCAD Co-design for a Competitive Advantage	John McMillan, Mentor	PCB Design/Layout/ Placement
12:00pm – 1:00pm LUNCH-N-LEARN, *Sponsored by Streamline Circuits (Tuesday conference attendees only)*		
1:00pm - 3:00pm		
11: Power Integrity & Decoupling Primer for PCB Designers	Ralf Bruening, Zuken	SI/PI
12: Laying Out Analog/Digital Planes	Robert Hanson, Americom	SI/PI
1:00pm - 4:30pm		
13: Effective PCB Design: Techniques to Improve Performance	Daniel Beeker, NXP Semiconductor	PCB Design/Layout/ Placement
14: Circuit Grounding to Control Noise and EMI	Rick Hartley, RHartley Enterprises	EMI/EMC & PCB Design
3:00pm - 5:00pm		
15: Thermal Integrity within an Electrical Design Flow	Jim DeLap, Ansys	PCB Design/Layout/ Placement
16: How to Fight Magnetic Noise Gremlins	Keven Coates, Geospace	EMI/EMC

WEDNESDAY, SEPTEMBER 12

8:00am CONFERENCE COFFEE BREAK, *Sponsored by Sierra Circuits*		
8:30am - 12:00pm		
17: The Complexities of Fine Pitch BGA Design	Susy Webb, Fairfield Industries	PCB Design/Layout/ Placement
9:00am - 10:00am		
18: PCB Reverse Engineering Countermeasures	Jeremy Hong, Hong's Electronics	PCB Design/Layout/ Placement
9:00am - 11:00am		
19: Multi-Board Design: Castellation, Connection, SI, Alignment	Chris Carlson and Alexey Sabunin, Altium	PCB Design/Layout/ Placement
20: An Intuitive Approach to Understanding Basic High-speed Layout	Keven Coates, Geospace	SI/PI
21: A Beginner's Introduction to PCB Trace Impedance	Ken Taylor, Polar Instruments	PCB Design
9:00am - 5:00pm		
22: Cost Reduction through Design for Manufacturing and Assembly	Gary Ferrari, FTG Circuits	DfF/DfM/DfA/DfT
23: The Complete Guide to Understanding Transmission Lines	Robert Hanson, Americom	High Speed

REGISTER NOW!

WEDNESDAY, SEPTEMBER 12 (continued)

TITLE	SPEAKER	CATEGORY
10:00am – 6:00pm EXHIBITION FLOOR OPEN		
10:00am – 2:00pm EXHIBIT HALL BOOTH BARISTA, *Sponsored by Zuken*		
10:00am - 12:00pm		
24: iPhone X – Steve Jobs' iPhone	Bill Cardoso, Creative Electron	PCB Design/Layout/ Placement
12:00pm – 1:00pm LUNCH ON EXHIBIT FLOOR, *Sponsored by Sierra Circuits*		
1:00pm - 3:00pm		
28: Thermal Design Considerations for SMD PCBs	Keven Coates, Geospace	PCB Design/Layout/ Placement
29: Signal Attenuation in Very High Speed Circuits	Rick Hartley, RHartley Enterprises	High Speed/PCB Design
1:00pm - 4:30pm		
30: HDI Routing Solutions	Susy Webb, Fairfield Industries	PCB Design/Layout/ Placement
31: The Basics of PCB Fabrication (101)	Paul Cooke, FTG Circuits	Fabrication
3:00pm - 5:00pm		
32: Differential Pair Routing for SI Control	Rick Hartley, RHartley Enterprises	High Speed/PCB Design
33: Evaluating the VIA Transition through TDR Simulation	Richard Villamor Legaspino, Analog Devices	RF/Microwave/PCB Design

FREE WEDNESDAY, SEPTEMBER 12

9am - 11:00am		
F1: Routing & Termination for Control of Signal Integrity	Rick Hartley, RHartley Enterprises	High Speed/PCB Design
9am - 10:00am		
F2: HDI: High Density Interconnect	Chris Nuttall, NCAB Group	PCB Design/Fabrication
10:00am - 11:00am		
F3: AI and Machine Learning Disrupting the Manufacturing of Your Products	Albert Yanez, AsteelFlash	Automation/Process Improvement
11:00am - 12:00pm		
KEYNOTE: Is Past Prologue? The Future of the PCB Design Industry - Walden Rhines, CEO, Mentor		
F4: Designing in the Age of Prototypes	Milan Shah, Royal Circuits	PCB Design
1:00pm - 2:00pm		
F5: Industry 4.0 and IPC-2581	Hemant Shah, IPC-2581 Consortium	Electronics Data Transfer/Standards
1:00pm - 3:00pm		
F6: The 10+ 21 Most Common Design Errors Caught by Fabrication (and How to Prevent Them)	David Hoover, TTM Technologies	DfF/DfM/DfA/DfT
2:00pm - 3:00pm		
F7: Efficient PCB Interposer Design Using a Novel Smart Router Based on Neural Networks and Genetic Algorithms	Xiao Ming Gao, Intel	PCB Design
3:00pm - 4:00pm		
F8: Optimizing Hardware for Your IoT Solution	Sean Priddy, Creation Technologies	Business/Markets
F9: PANEL: The Future of PCB Engineers	Phil Marcoux, PPM, Moderator	3D Printing/Fabrication
4:00pm - 5:00pm		
F10: 3D Printed Electronics: A New Dimension in Prototyping & Manufacturing	Simon Fried, Nano Dimension	Printed Electronics
F11: PANEL: Understanding the AS9100D Standard	Peter Bigelow, IMI, Moderator	Standards

CAD TOOL CORNER – FREE – WEDNESDAY, SEPTEMBER 12

1:00pm - 2:00pm		
C1: Ensure Your Electronic Design is Reliable and Robust by Simulation – During Schematic, Before Manufacturing and Testing	Yizhak Bot, BQR	PCB Design

CAD TOOL CORNER – FREE – WEDNESDAY, SEPTEMBER 12 - Continued

2:00pm - 3:00pm		
C2: Retargeting Your Libraries for Newer, Better Processes without Breaking Your Bank	Vince Di Lello, Cadence Design Systems	PCB Design/Layout/ Placement
3:00pm - 4:00pm		
C3: Designing PCBs in the Context of a System	Gary Hinde, Cadence Design Systems	PCB Design
4:00pm - 5:00pm		
C4: Multi-Domain Collaboration for Electronics Systems Design	David Wiens, Mentor	PCB Design

THURSDAY, SEPTEMBER 13

TITLE	SPEAKER	CATEGORY
8:00am CONFERENCE COFFEE BREAK, *Sponsored by Sierra Circuits*		
8:30am - 12:00pm		
34: Design of Power Distribution and Decoupling	Rick Hartley, RHartley Enterprises	EMI/EMC & SI/PI & PCB Design
35: Part Placement Choices and Consequences	Susy Webb, Fairfield Industries	PCB Design/Layout/ Placement
9:00am - 10:00am		
36: Intelligent DfM for Assembly	Kevin Webb, Mentor	PCB Design/Layout/ Placement
37: Providing Solutions for Thermal Management within RF Designs	James Barry, PCB Technologies	RF/Microwave/Thermal Management
9:00am - 11:00am		
38: The Mystery of Bypass Capacitors	Keven Coates, Geospace	SI/PI
39: Ask the Flexperts – Flexible Circuit Design through Test with Lessons Learned	Mark Finstad, Flex Circuit Technologies, and Nick Koop, TTM Technologies	PCB Design & Fabrication Processes
9:00am - 12:00pm		
40: Designing Embedded Passives and Related Technologies	Gary Ferrari, FTG Circuits	Embedded Passives/ Fabrication/Components
10:00am - 11:00pm		
41: DfM: Getting It Right from the Start	Chris Nuttall, NCAB Group	DfF/DfM/DfA/DfT
42: Arriving at an Optimal Stackup for Printed Circuit Boards Used in Silicon Validation	Vijay Nanjai Anandan, Tessolve Semiconductor	Fabrication
11:00am - 12:00pm		
43: Leveraging 3-D Layout to Optimize Rigid-Flex Designs	Vern Wnek, Mentor	PCB Design/Layout/ Placement
44: Overview of Several RF Structures and How They Work	John Coonrod, Rogers	RF/Microwave/PCB Design
12:00 pm – 1:00 pm LUNCH-N-LEARN, *Sponsored by Polar Instruments (Thursday conference attendees only)*		
1:00pm - 3:00pm		
45: Electromagnetic Fields for Normal Folks: Show Me the Pictures and Hold the Equations, Please!	Daniel Beeker, NXP Semiconductor	EMI/EMC
1:00pm - 4:30pm		
46: Flexible and Rigid-Flex Circuit Design and Assembly Process Principles	Vern Solberg, Solberg Technical Consulting	DfF/DfM/DfA/DfT
47: Best DfM Practices for Board Engineers	Susy Webb, Fairfield Industries	PCB Design/Layout/ Placement
48: RF and Mixed Signal Board Design	Rick Hartley, RHartley Enterprises	RF/Microwave/PCB Design
3:00pm - 5:00pm		
49: PCB Design Techniques to Improve ESD Robustness	Daniel Beeker, NXP Semiconductor	EMI/EMC
1:00pm - 4:00pm		
50: PCB Layout: Place and Route	Mike Creeden, San Diego PCB	PCB Design

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TUESDAY, SEPTEMBER 11

8:00 am CONFERENCE COFFEE BREAK, Sponsored by Sierra Circuits

8:30 AM – 12 NOON

1: PCB DESIGN STRATEGY FOR HIGH DENSITY BGA AND CSP COMPONENTS

Vern Solberg, Solberg Technical Consulting

The ball grid array and chip-scale package families of components are recognized by many as the best solution for meeting the space restrictions of next-generation portable and handheld electronic products, but companies are also expecting improvements in functionality and performance. Because of the higher terminal density of BGA, fine-pitch BGA and CSP, PCB designers have realized the implementation of proven design rules ensures a positive effect on PCB fabrication yield, assembly process efficiency and end product cost. Furthermore, attendees will be able to explore a number of alternative 2.5-D and 3-D semiconductor packaging methodologies, review manufacturers design guidelines and assess alternative assembly process variations for HDI applications. This half-day tutorial will include a study of land pattern geometry options, HDI circuit routing guidelines, as well as the important factors related to specifying base materials and surface finishes that are most compatible with high-volume automated assembly processing. Participants will also have an opportunity to review and discuss JEDEC packaging standards for array configured components, the latest version of the IPC-7094, "Die Size and Flip-Chip BGA Design Standard," and IPC-7095, "BGA Design Standard," a document that includes both wide and fine-pitch array packaging methodology. Topics covered: 1. BGA/CSP process technologies and standards; single die package-level assembly variations; 2-D and 3-D multiple die package methodologies; JEDEC standards for BGA and CSP; IPC standards for implementing BGA and CSP. 2. PCB design guidelines for BGA and CSP; component selection and surface area planning; evaluating BGA and CSP terminal variations; land pattern development for array configured components; circuit routing strategies for BGA and CSP. 3. HDI circuit and Microvia design implementation; defining circuit complexity classifications (IPC-2226); analysis and consideration when estimating circuit density; benefits for implementing blind and buried microvias; guidelines for stacked, staggered and in-land microvias. 4. Specifying PCB base material, surface finish and coatings; reviewing established standards for circuit substrate materials; studying alternative high-performance material variations; choosing solder-compatible surface finishes for HDI circuits; specifying suitable solder mask coatings for the PCB. 5. Preparation for high-volume assembly processing; system requirements for BGA and CSP device placement; basic features needed for SMT assembly processing; palletizing to maximize assembly process efficiency; solder stencil development and solder alloy variations.

Who should attend: PCB Designer, System Designer, Hardware Engineer, Fabricator Engineer/Operator, Assembly Engineer/ Operator, Test Engineer

Target audience: Beginner, Intermediate

9:00 AM TO 11:00 AM

2: LAYOUT OF SWITCH MODE POWER SUPPLIES

Rick Hartley, Rick RHartley Enterprises

When executing PCB layout, we tend to treat digital circuits differently from analog circuits. Each has its own critical requirements. Switch mode power supplies are another wrinkle altogether and usually need to be treated differently from either analog or digital structures. All switch mode power supplies have four to five circuit loops, all of which are important, but a couple of these loops are downright critical in terms of PCB layout. An improperly designed switch mode supply often will not function as intended, and in some cases, not at all. In contrast, understanding what makes up a switcher circuit and knowing how to take care of the loops during PCB layout will allow these supplies to operate flawlessly, and with very high efficiency.

This course will outline the difference between switchers and series-regulated supplies, the different types of switcher circuits (buck, boost, etc.), basic theory of operation of switcher circuits and the impact of the various components, definition and behavior of the five loops, layout to isolate loops from one another to minimize voltage drop and to control current paths, layout to minimize noise and EMI, effect of paralleling output capacitors and proper grounding technique.

Who should attend: PCB Designer, Circuit/Hardware Engineer, SI Engineer, System Engineer

Target audience: Intermediate

3: POWER DISTRIBUTION MADE EASY

Daniel Beeker, NXP Semiconductor

This presentation will present a simple EM physics and geometry-based approach to designing power distribution networks on PCBs. From input power connection to the IC die, the simple rules discussed can be used to reduce power supply noise and improve EMC.

Who should attend: PCB Designers, System Designers, Hardware Engineers, SI Engineers

Target audience: Beginner, Intermediate

9:00 AM TO 5:00 PM

4: THE BASICS OF PCB DESIGN

Susy Webb, Fairfield Industries

Technical sessions at conferences often emphasize the latest techniques and technologies, but those classes are often too in-depth for a novice designer, and don't speak to the questions from the engineers who need to design their own boards. This class features an overview of the entire process of designing a board, from start to finish. We will begin with creating manufacturable footprints that meet the IPC specs. Then we will address some common placement techniques like floor planning, color coding, flow, orientation, and placement to set up routing. We will follow that with a discussion of planes and stackups and how to configure them to get the best results for parts and signals. Next, we move on to some fanout and routing techniques that are helpful for completing the design connections to meet the number one design rule: good electrical performance. We will complete the process by discussing some manufacturability concerns that can be affected by the way the board is designed, some finishing issues, and sending out good documentation that the manufacturers can easily understand and use.

Who should attend: PCB Designer

Target audience: Beginner

5: WHAT'S NEW IN THE IPC DESIGN STANDARDS, AND HOW TO USE THEM

Gary Ferrari, FTG Circuits

Designers are under pressure to not only lay out a circuit board to meet functional requirements, but produce a cost-effective design that meets the requirements of fabrication, assembly, test, and field service. As a result, designers must keep up with the latest changes/additions to the industry standards they must use. IPC has shortened the development cycle for many of its standards. This session will identify a minimum set of standards

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that the designer should be familiar with. Highlighted will be recent important changes to the most used design, materials, fabrication, assembly and test standards. The changes are **significant,** and affect all classes of products.

Attendees will learn recommended minimum standard set for designers, standards that affect the design of printed boards, and design changes that affect manufacture and reliability of a product.

Who should attend: PCB Designer, Electrical Engineer
Target audience: Beginner, Intermediate

6: PCB STACKUP DESIGN AND MATERIALS SELECTION

Bill Hargin, Z-zero

The objective of this tutorial is to guide design teams through the process of evaluating and selecting the right laminate for a design, creating PCB stackups that meet the requirements of complex, multilayer boards that work right the first time, within budget, and with reproducible results across multiple fabricators. The course will go into detail on tradeoffs between loss and cost, including dielectric loss, resistive loss, surface roughness, as well as glass-weave skew. After attending this course, students will be knowledgeable of PCB laminate tradeoffs, the laminate-materials market, and the process of troubleshooting problematic stackup designs. Attendees will also be exposed to cost-effective strategies for controlling loss and glass-weave skew.

Who should attend: PCB Designer, System Designer, Hardware Engineer, SI Engineer, Fabricator Engineer/Operator, Other
Target audience: Beginner, Intermediate, Advanced

7: TROUBLESHOOTING AND DEFECT RESOLUTION OF SMT ASSEMBLY PROCESSES

Jim Hall and Phil Zarrow, ITM Consulting

We don't assemble electronics in a perfect world. Defects happen. This course examines failures and root cause analysis of PCBA defects, starting with a clear definition of the generic types of defects and their impact, such as non-function, reduced reliability, etc. Detection and determination methodologies and procedures will be discussed. Attributes of specific processes and equipment centers, as well as materials that can contribute to defect generation are identified. Specific defects are then analyzed using these background methodologies: type of defect and impacts, detection methods, possible contributing causes, etc. Finally, general strategies and guidelines for preventing defects will be presented. This seminar is for anyone involved in directing, developing, managing and/or executing failure and root cause analysis and defect resolution, including managers, engineers and others in manufacturing, quality and design.

Who should attend: Hardware Engineer, Assembly Engineers/ Operator, Test Engineer
Target audience: Beginner, Intermediate

10:00 AM – 11:00 AM

25: CONTINUING TEST POINT MANAGEMENT THROUGHOUT A PCB DESIGN FLOW

Mark Laing, Mentor

At PCB West 2017 I presented how design for test (DfT) needed to become proactive in the PCB design flow. This paper focused on starting DfT analysis as part of the schematic capture phase and not leaving it until late in the layout phase. This presentation will continue this theme, and discuss how PCB layout can further enable improvements in testability and DfT, with ongoing test point management as the next logical step from schematic capture. Existing layouts will be reviewed for testability coverage to find ways they can also be improved in subsequent design revisions.

Who should attend: PCB Designer, Fabricator Engineer/Operator, Assembly Engineer/Operator, Test Engineer
Target audience: Intermediate

11:00 AM – 12:00 NOON

8: MANAGING YOUR IMPEDANCE, COUPLING AND RETURN PATHS IN DESIGN AND AVOID UNNECESSARY ITERATIONS WITH SI/PI ENGINEERS

Dennis Nagle, Cadence Design Systems

Are you fixing high-speed issues on your design by iterating with your SI/PI engineers? There is a better way. This talk will describe how PCB designers can screen their designs and identify issues that can avoid impedance mismatch, crosstalk and return path issues before SI/PI analysis.

Who should attend: PCB Designer
Target audience: Beginner, Intermediate, Advanced

9: EVALUATING AN APPROPRIATE POWER PLANE THROUGH POWER INTEGRITY SIMULATION

Richard Villamor Legaspino, Analog Devices

Most automatic test equipment (ATE) final test boards have analog and digital devices. These devices may be operation amplifier (OP-Amp IC), transistors and memory ICs, which require an appropriate power plane PCB design to connect from voltage source to the load devices. The power plane layout must be carefully designed to prevent power integrity issues such as current-resistance (IR) drop, plane current density, power plane density and power plane impedance. The other way to validate these issues is through power integrity simulation. Simulation can be performed at the pre- or post-layout design stage to prevent any respins of the board. In this presentation, the speaker used the Power-DC and Optimize-PI simulation tool to evaluate the appropriate power plane topology. To measure the IR drop, plane current density, power plane density and power plane impedance of the power plane layout.

Who should attend: PCB Designer, SI Engineer, Assembly Engineer/ Operator
Target audience: Intermediate

27: ECAD-MCAD CO-DESIGN FOR A COMPETITIVE ADVANTAGE

John McMillan, Mentor

Many design teams struggle to reduce product development schedules and improve time-to-market. In a recent survey, the need to improve time-to-market was identified as a primary business objective, ahead of the need to reduce product cost and improve product quality. Asked about initiatives to accelerate time-to-market, the leading response was to improve communication and collaboration across engineering. If you were to push down further into a methodology to implement this initiative, you would find that improving ECAD-MCAD collaboration not only reduces product development time, thereby improving time-to-market, it also provides a sustainable competitive advantage for your design team. During this session we will discuss how an efficient ECAD-MCAD co-design process can be an enabler for design teams to eliminate costly electro-mechanical issues during new product development. We will look at the innovative solutions available in the latest generation of software technology and how they can help your team obtain a sustainable competitive advantage. Recommended best practices and a summary of the benefits associated with an optimized ECAD-MCAD collaboration process will be reviewed and discussed.

Who should attend: PCB Designer, Other
Target audience: Beginner

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12:00 noon – 1:00 pm LUNCH-N-LEARN, Sponsored by Streamline Circuits

1:00 PM – 3:00 PM

11: POWER INTEGRITY & DECOUPLING PRIMER FOR PCB DESIGNERS

Ralf Bruening, Zuken

The evolving requirements of new electronic applications in various markets (e.g., automotive, communication, IoT) are forcing engineers to an ongoing improvement of their design processes. The overall performance and the EMC behavior of such electronic systems are determined not only by the design of the circuitry, layout geometry and the IOs, but more these days by the power distribution networks (PDNs). Strict reliability requirements and lack of real estate on such complex systems often prevent first order power integrity countermeasures from the past (e.g., sprinkling the board with 100nF caps). Today's supply voltage decrease with every new silicon generation is contributing to the problem domain in the same amount as the common goal of reducing power consumption of electronic systems does. This and the resulting shrinking noise margins for new ICs define increasing demands for the quality and stability of power supply systems. Hence, tighter requirements and constraints from silicon vendors are defined for the power supply the PCB designers have to follow – in conjunction with tougher decoupling schemes. In this session requirements and the basic of PCB power distribution systems are explained. Issues like plate capacitance, loop inductances and cavity resonance are explained without deep math. Side effects to the signal integrity and EMC domains are shown using illustrated practical examples. Guidelines for a first order covering and resolving power integrity issues are given regardless of the used PCB-design and ECAD process. The how and why of decoupling will be illustrated covering in detail the role of bypass capacitor. Power integrity simulation capabilities will be explained and demonstrated in a generic vendor-neutral manner as a potential problem-solving approach, together with silicon vendor support documents (i.e., constraint and spreadsheet tools) addressing power integrity issues as an essential part of a state-of-the-art PCB design process. Examples from various industries (e.g., automotive) will complement the session with excerpts from practical application experience.

Who should attend: PCB Designer, System Designer, Hardware Engineer, SI Engineer, Test Engineer

Target audience: Beginner, Intermediate

12: LAYING OUT ANALOG/DIGITAL PLANES

Robert Hanson, Americon

This tutorial will discuss the properties behind ground. This tutorial will address the following questions and more: Which should be used for your design – ground, modified or multipoint ground? What causes near-end and far-end crosstalk, and how is it measured and simulated? Why are solid ground planes best? What is intelligent parts placement, and what is its effect on ground return current? Attendees will learn about the concept of moats/floats/drawbridges, how to layout split planes – CMOS/TTL, PECL, and analog using different biases and also controlling crosstalk, characteristic impedance and cost in 4, 6, 8, and 10-layer stackups using the same bias voltage; how to stack printed circuit board layers (e.g., 4, 6, and 10-layer for Zo and crosstalk control; copper fills on signal layers, minimizing warpage; interplane capacitance: material thickness and selection and stackup placement; SIR vs frequency; software for performing crosstalk; ground bounce tests.

Who should attend: PCB Designer, System Designer, Hardware Engineer, SI Engineer

Target audience: Intermediate

1:00 PM – 4:30 PM

13: EFFECTIVE PCB DESIGN: TECHNIQUES TO IMPROVE PERFORMANCE

Daniel Beeker, NXP Semiconductor

As IC geometries continue to shrink and switching speeds increase, designing electromagnetic systems and printed circuit boards to meet the required signal integrity and EMC specifications has become even more challenging. A new design methodology is required. Specifically, the utilization of an electromagnetic physics-based design methodology to control the field energy in your design will be discussed. This training module will walk through the development process and provide you with guidelines for building successful, cost-effective printed circuit boards.

Who should attend: PCB Designer, System Designer, Hardware Engineer, SI Engineer

Target audience: Beginner, Intermediate

14: CIRCUIT GROUNDING TO CONTROL NOISE AND EMI

Rick Hartley, RHartley Enterprises

When a time-varying (AC) current flows, state-changing electric and magnetic fields are present. These fields, when not controlled, are the source of noise and EMI. In recent years, ICs with very fast rise-time outputs have made problems common, even in circuits clocked at low frequencies. Knowing all the basics of proper grounding can contain and control stray fields, making noise and EMI issues virtually nonexistent.

This course will cover the concept of "ground," location of fields in the PCB, when is a circuit a waveguide, where high- and low-frequency currents flow, keys to controlling common mode EMI, cables and other radiators, source control of EMI, effects of IC style and packaging, impact of connector pin-out, effect of component positions on EMI, planes and plane islands in the PCB (to split or not to split ground), routing to control noise, routing and the I/O structure, board stack-up, I/O filtering and blocking for single-ended and differential lines.

Who should attend: PCB Designer, Circuit/Hardware Engineer, SI Engineer, System Engineer

Target audience: Intermediate

3:00 PM – 4:00 PM

15. THERMAL INTEGRITY WITHIN AN ELECTRICAL DESIGN FLOW

James DeLap, Steven G. Pytel Jr. and Mehdi Abarham, Ansys

Modern design requirements necessitate a workflow that allows for free-flowing information and iterations between electrical, thermal, and mechanical design teams. This workshop will explore new simulation tools that enable electrical and thermal co-design and optimization, as well as showcasing best practices for dealing with electrical and mechanical CAD (ECAD and MCAD) files. The workshop targets electrical engineers, providing them an overview of basic thermal dynamics, heat transfer modes, power delivery/consumption optimization in ECAD/MCAD, while keeping the focus on how to identify problematic designs early, thereby creating a collaborative working environment with mechanical engineers.

Who should attend: PCB Designer, System Designer, Hardware Engineer

Target audience: Intermediate

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3:00 PM – 5:00 PM

16: HOW TO FIGHT MAGNETIC NOISE GREMLINS

Keven Coates, Geospace

Have you ever had a noise-sensitive circuit and tried to find the noise source? Even after you completely encased sensitive portions in all sorts of shielding, you still had noise? It's very possible this is magnetic noise. Lower frequency magnetic fields can't be contained and shielded against in the same way electric fields can. In this presentation, hear about the author's nine-month long battle with a specific magnetic noise issue, the best tools to fight it, twisted pair, current loops, and the best ways to test for and defeat magnetic noise in your designs.

Who should attend: PCB Designer, System Designer, Hardware Engineer, SI Engineer

Target audience: Beginner, Intermediate, Advanced

WEDNESDAY, SEPTEMBER 12

8:00 am CONFERENCE COFFEE BREAK, Sponsored by Sierra Circuits

8:30 AM – 12 NOON

17: THE COMPLEXITIES OF FINE PITCH BGA DESIGN

Susy Webb, Fairfield Industries

Designing with BGAs is much more challenging than in the past! The ball pitches are going down, and the total pin counts and package size are going up, making everything more complex. With those changes, the signal integrity and EMI issues become more profound; the fanout and routing are much more challenging, and the power connections more difficult. Add to that the manufacturing concerns that have surfaced from small pad openings and tiny capacitors, and the designer has to face some real complex issues. In this presentation, we will discuss all of those things and more, including choosing effective BGAs, placement for components and caps, grid systems for parts and routing, through-hole and microvia fanout possibilities, and some manufacturing issues unique to these kinds of designs. This class has a lot of illustrations and examples!

Who should attend: PCB Designer

Target audience: Beginner, Intermediate, Advanced

9:00 AM TO 10:00 AM

18: PCB REVERSE ENGINEERING COUNTERMEASURES

Jeremy Hong, Hong's Electronics

Designing circuits and laying out a printed circuit board (PCB) can be a complicated and intensive process. Design engineers use many shortcuts and tricks to cut costs and time of development. As it turns out, many of these shortcuts and tricks can lead to security flaws in a product. Working on both sides, design and reverse engineering, it has been found that implementing security and countermeasures on PCBs are the last priority for design engineers – and sometimes totally ignored. This is apparent in the design of IoT (Internet of things) devices. This presentation points out some fundamental aspects of the hardware design engineering process that can lead to hardware vulnerabilities.

Who should attend: PCB Designer, System Designer, Hardware Engineer, Test Engineer

Target audience: Beginner, Intermediate

9:00 AM TO 11:00 AM

19: MULTI-BOARD DESIGN: CASTELLATION, CONNECTION, SI, ALIGNMENT

Chris Carlson and Alexey Sabunin, Altium

Aesthetics, ergonomics and industrial form are paramount design objectives, as new products must appeal to attention-starved consumer audiences. Intelligent people increasingly crave intelligent products. The desire to maximize production efficiency by consolidating all the electronics onto one board is at odds with higher mechanical design priorities. Add to that the desire markets inherently develop for configurations and optional extras, and it's hard to avoid a multi-board design approach. This technical session presents practical approaches to multi-board system-level PCB design, including partition boundaries, subcircuit relocation, interconnect methods, panels and layer stacks, and mechanical integration with enclosure design. We will also cover potential disaster areas and ways to avoid pitfalls, how to effectively manage connectivity, and improve manufacturing outputs for unambiguous fabrication and assembly. Specific topics discussed will be multiboard methodologies overview; partitioning; connectors for board to board; castellated module design approach for IPC-A-610G quality compliance; multiboard signal and power integrity issues; module form factor overview pros and cons; connectivity management and signal probing; 3-D mechanical integration and assembly management. Methods presented in this workshop are extensible and applicable to any toolset or workflow.

Who should attend: PCB Designer, System Designer, Hardware Engineer, SI Engineer

Target audience: Beginner, Intermediate, Advanced

20: AN INTUITIVE APPROACH TO UNDERSTANDING BASIC HIGH-SPEED LAYOUT

Keven Coates, Geospace

What is a wire? At high speeds, it behaves very differently from what we were taught in college! This is a presentation on high-speed basics that helps make the subject intuitive in a way that's never been presented before. Learn about how frequency enters the picture, high-speed signal propagation, impedance, noise, and reflections with easy-to-understand animations and analogies to understand this subject on a deeper level.

Who should attend: PCB Designer, System Designer, Hardware Engineer

Target audience: Beginner

21: A BEGINNER'S INTRODUCTION TO PCB TRACE IMPEDANCE

Ken Taylor, Polar Instruments

What is impedance anyway, what causes it, why does it matter, and what happens if we get it wrong? This entry-level presentation describes the component properties of a PCB trace (a transmission line) that come together to determine the impedance. Maybe surprisingly, impedance is experienced in various other forms every day, probably every minute of every day. Most people never thought of it that way. This presentation begins by briefly identifying and acknowledging those experiences, and relates them to the electrical transmission line and its component parts and their characteristics. Next, it looks at the transmitted signal as it progresses from the signal source into the line, as it propagates along the line, and what happens when it eventually reaches the end of the line – depending on how the line is terminated: open/short/matched/mismatched. The mathematics will be kept simple, nothing worse than x = a.y or similar and, of course, the good old square root. A brief review of frequency-dependent problems

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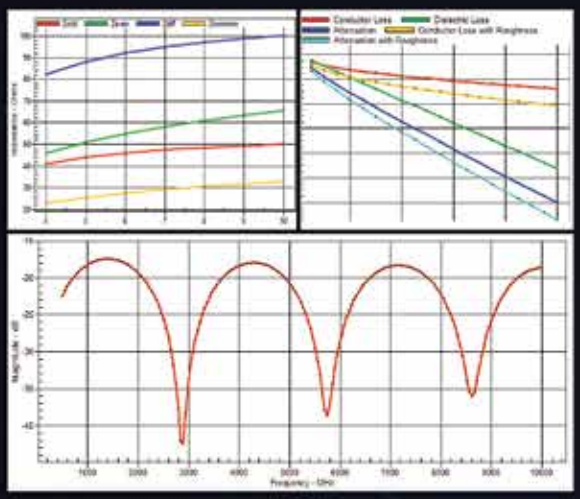
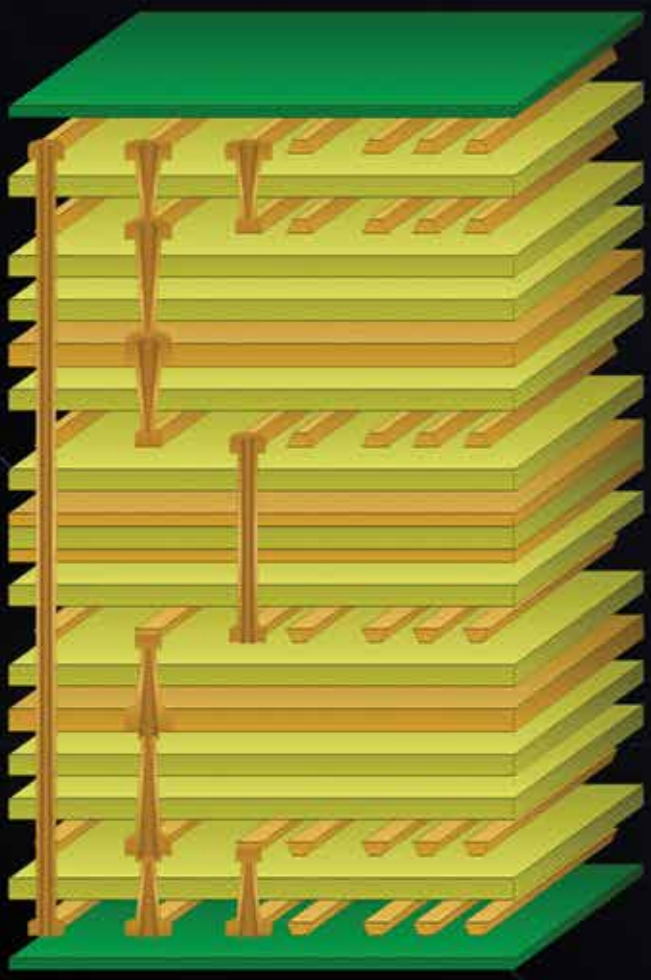
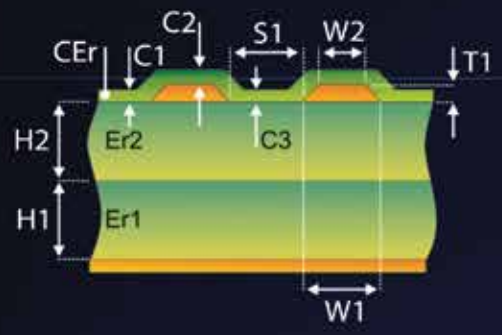




Impedance Measurement

Copper Roughness

Insertion Loss



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of dielectric loss (signal energy lost to the line's surrounding environment) and copper loss (signal energy lost to the copper conductor) might be included.

Who should attend: Fabricator Engineer/Operator, Assembly Engineer/Operator, Other

Target audience: Beginner

9:00 AM – 5:00 PM

22: COST REDUCTION THROUGH DESIGN FOR MANUFACTURING AND ASSEMBLY

Gary Ferrari, FTG Circuits

Technologies such as lead-free, small pitch BGAs, microvias, embedded passives, controlled impedance, and EMI present manufacturing challenges that must be addressed by today's designers, not to mention increased costs. It is easy to blame escalating costs on these technologies. Much of the blame may be attributed to a lack of understanding of the manufacturability rules associated with these technologies, however. Designers should be designing for the most cost-effective product without sacrificing performance.

Cost reduction, by design, forms the fundamental building blocks for this session. This session will be divided between lectures and interactive discussion groups. These groups will explore, under guidance, material issues for lead and lead-free environments, high performance, HDI, assembly, and surface finishes for various environments. There will be ample time allocated to look at individual challenges faced by the attendees.

Attendees will gain a clear understanding of overall DfM issues, cost drivers, how to apply DfM concepts to specific designs, and the notes that should be placed on fabrication drawings.

Who should attend: PCB Designer, Electrical Engineer

Target audience: Intermediate, Advanced

23: THE COMPLETE GUIDE TO UNDERSTANDING TRANSMISSION LINES

Robert Hanson, Americon

Fundamentals • Frequency, time, and distance • Lumped versus distributed systems • EM fields • Geometry, C, L, and Zo interrelationships • C&L resonance transmission line characteristics • The quality factor, Q, and why lumped circuits can ring and cause EMI • Infinite uniform transmission line • Effects of source and load impedance • Special transmission line cases • Determining line impedance and propagation delay using TDR and VNA • Skin/proximity effect and dielectric loss • The capacitive load: Zo and propagation delay • Matching Zo with trace alterations (neck-downs): minimizing the C load • 90°, 45° bends: are they concerns? • Characteristics of T lines: coax, pair, micro strip, buried micro strip, stripline and differential: asymmetric, dual, edge.

Who should attend: PCB Designer, System Designer, Hardware Engineer, SI Engineer

Target audience: Intermediate

10:00 am – 6:00 pm EXHBITION FLOOR OPEN

10:00 am – 2:00 pm BOOTH BARISTA, Sponsored by Zuken

10:00 AM – 12:00 NOON

24: IPHONE X – STEVE JOBS' IPHONE

Bill Cardoso, Creative Electron

It's been 10 years since Steve Jobs introduced the iPhone to the world. Much has happened since then. Over this past decade, the iPhone became a reference design, and the object of desire of a legion of fans who wait anxiously for every launch of the Cupertino company. Undoubtedly, the most advanced iPhone on the market today, the iPhone X is a technology marvel. The double-stacked boards, dual battery, and a face recognition sensor bring the iPhone X to a whole different level. In this presentation, we'll explore these technological advances during a live teardown of the iPhone X. The teardown will be followed by detailed coverage of the technical details of critical parts of the device. This live teardown will be accompanied by x-ray and CT images of the iPhone X, so the audience will get unprecedented insights on what makes this iPhone tick. More important, we will explore the assembly process utilized to put the iPhone X together. This presentation is targeted at a wide technical audience looking for a better understanding on how advanced consumer electronics are designed and assembled.

Who should attend: System Designer, Hardware Engineer, SI Engineer, Fabricator Engineer/Operator, Assembly Engineer/Operator, Test Engineer

Target audience: Beginner

12:00 noon – 1:00 pm LUNCH on the Exhibit Floor, Sponsored by Sierra Circuits

1:00 PM – 3:00 PM

28: THERMAL DESIGN CONSIDERATIONS FOR SMD PCBS

Keven Coates, Geospace

By now everyone has seen those nice aluminum core PCBs that dissipate heat fantastically, but what do you do when all you have to work with is FR-4 and SMD components? How do you keep those MOSFETs and faster processors cool? How are semiconductor packages designed to dissipate heat? What's the best way to utilize that? This class will cover understanding thermal resistance, how airflow affects things, good design goals, estimating junction temperature, and how to pick the right components to minimize the temperature of your design and therefore maximize reliability.

Who should attend: PCB Designer, System Designer, Hardware Engineer

Target audience: Beginner, Intermediate

29: SIGNAL ATTENUATION IN VERY HIGH SPEED CIRCUITS

Rick Hartley, RHartley Enterprises

In all high-speed/high-frequency circuits, signal integrity is dependent on a number of variables, all of which accumulate to impact the noise budget of the circuit. With very high-speed circuits, an even larger number of issues come into play, and all the effects are more extreme. Some problems are driven by design deficiencies, some by the physical structure and design of the ICs, and still more are driven by the PCB's copper style and base material parameters.

This course will outline all the effects impacting signal integrity at very high speeds and will detail such items as via stubs, jitter, inter-symbol interference, impact of copper style on skin effect, loss tangent, impact of layer change during routing and other major signal integrity concerns, as well as the impact some of these items have on timing and the Y-axis attenuation of signal eyes. Also discussed will be solutions to these issues, including some excellent high-speed base materials.

Who should attend: Circuit/Hardware Engineer, SI Engineer, PCB Designer, System Engineer

Target audience: Intermediate, Advanced

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1:00 PM – 4:30 PM

30: HDI ROUTING SOLUTIONS
Susy Webb, Fairfield Industries

With the pitch of parts getting smaller and pin count getting larger, there is a need to get as much routing as possible into very small areas of the PCB. HDI will help accomplish this, but the technology requires some different setup and thought as to what is needed. One has to decide on design priorities, complexity needed, cost required or allowed, the type and size of vias, best via patterns to use, and how signals, power and ground will move from one layer to another. Additionally, the layer structure, impedance, signal return, and layer paired routing all must be considered for signal integrity and EMI control, and a general understanding of manufacturability is needed. We will discuss all those things, the electronics involved, different ways to accomplish the routing, and offer many examples and pictures of how to work with them to reach our goals.

Who should attend: PCB Designer
Target audience: Beginner, Intermediate, Advanced

31: THE BASICS OF PCB FABRICATION (101)
Paul Cooke, FTG Circuits

With ever-decreasing geometries and increased density, today's PCBs are extremely complex. This seminar looks at how a PCB is fabricated, and the challenges the fabricator faces to achieve the design intent and meet the customer and industry standards. We will examine the processes needed to form microvias, image µBGAs, plate copper in holes the thickness of a human hair, and select surface finishes needed for very fine-pitch components. The half-day seminar will be interactive to ensure all questions related to PCB fabrication are answered.

Who should attend: PCB Designer, Fabricator Engineer/Operator, Assembly Engineer/Operator, Test Engineer
Target audience: Beginner

3:00 PM – 5:00 PM

32: DIFFERENTIAL PAIR ROUTING FOR SI CONTROL
Rick Hartley, RHartley Enterprises

Differential pairs have been used in PCBs for years to carry high-speed serial and high-speed parallel data, in a variety of bus formats. Many board designers and engineers believe the rules for differential pairs are the same in a printed circuit board as they are in a cable or a twisted pair of wires. This is not the case!

This course will cover the advantages of differential pairs vs., single-ended lines, which differential pair format gives the best impedance control, what is the right spacing between the lines of a pair, crosstalk between differential pairs, what's important in differential pair routing, how much skew (line length mismatch) is really acceptable, the impact of material type and the impact of vias on signal integrity and EMI.

Who should attend: Circuit/Hardware Engineer, SI Engineer, PCB Designer, System Engineer
Target audience: Intermediate

33: EVALUATING THE VIA TRANSITION THROUGH TDR SIMULATION
Richard Villamor Legaspino, Analog Devices

As PCBs become dense, routing high-speed digital (HSD) traces in a single layer has become complicated. Now most of the layout designs use at least two layers for routing these kinds of signals (RF and HSD). The speaker looks at the effects of having stubs in designs, and further improving it by removing the stubs and controlling the vertical interconnect access (VIA) using a 50 Ohm coaxial approach. Trace-to-vertical interconnect access (VIA) transition has been a common issue in high-speed digital PCB designs and applications. The speaker looks at the effects of having stubs in designs, and further improving it by removing the stubs and controlling the VIA using a 50 Ohm coaxial approach. The speaker explores the five different VIA transitions and the effects of each specific method applied to it using EMPro (electro-magnetic professional) FDTD (finite difference time domain) TDR (time domain reflectometry) simulation in correlation to an actual design. The speaker used a 3-D simulation tool, which is EMPro, using FDTD Solver for TDR and FEM (finite element method) for S-parameter analysis. The speaker fabricated a simple circuit board design using a micro-strip single-ended trace to via transition for correlation.

Who should attend: PCB Designer
Target audience: Intermediate

FREE WEDNESDAY

9:00 AM – 11:00 AM

F1: ROUTING & TERMINATION FOR CONTROL OF SIGNAL INTEGRITY
Rick Hartley, RHartley Enterprises

IC output rise time contributes more heavily to loss of signal quality than the clock frequency of the circuit. Since most ICs today have rise and fall times under 1.0 nanosecond, many engineers and printed circuit designers find themselves fighting signal integrity problems in circuits being clocked in the low to mid tens of megahertz. Traces on circuit boards with rapid rise and fall times are referred to as high-speed transmission lines. The single greatest contributor to signal integrity issues is the lack of proper routing of lines, lack of poor control of impedance and the lack of proper termination.

This course will focus on the issues PCB designers and engineers need to know when designing with today's "high-speed" components. Topics include: At what length a line is high speed, line length's effect on signal integrity when proper routing is not implemented, understanding and controlling line impedance, PCB material impact on impedance, long "Ts" in lines, routing schemes that work, when to terminate a line, proper termination of the line, when termination is not needed and board stack-up.

Who should attend: Circuit/Hardware Engineer, SI Engineer, PCB Designer, System Engineer
Target audience: Beginner, Intermediate

9:00 AM – 10:00 AM

F2: HDI: HIGH DENSITY INTERCONNECT
Chris Nuttall, NCAB Group

How do I get started with HDI? This session explains what defines an HDI board, standards, design rules, and driving forces for HDI.

Who should attend: PCB Designer, System Designer, Hardware Engineer, Test Engineer, Other
Target audience: Intermediate, Advanced

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10:00 AM – 11:00 AM

F3: AI AND MACHINE LEARNING DISRUPTING THE MANUFACTURING OF YOUR PRODUCTS

Albert Yanez, AsteelFlash

In manufacturing, we work systematically at ways to save time while maintaining the highest yields. This has been evident over the past 50 years, as methodologies were born that would help streamline operations and indoctrinate staff. These have helped form today's best practices, followed in every modern manufacturing company globally. These processes and systems can be seen in the assembly line, such as TQM (Total Quality Management), Six Sigma and Lean. We also know future products will be even more design savvy, with intricate and custom fabrication methods and materials. From diagnostics equipment through to the most advanced automotive systems, we could see what was needed to outpace, while providing no decrease in quality. Then, we considered the challenges our clients face forecasting, dealing with supply-chain concerns and distributing key materials as end-products require. We needed a manpower automation solution that could help with indirect labor and lend a hand in production. We wanted to automate indirect labor functions over time, with the goal of maturing into a 50/50 machine-to-human task force ratio. This would allow us to maintain a "mentor" role over the systems, while having an unlimited workforce on call. Today, we are in the early stages of bringing online portions of the intelligence and weaving them into the daily routines of current team members. Using Neural's proprietary methodologies, we targeted chunks of these identified networks, and follow system deployment processes to maintain quality adherence. To help with transformation, we utilize an advanced onboarding concept where we operate as a startup within our own company, consuming the processes internally via Smith (SM) (the Artificial Intelligence), to maintain control during the Neural Corps' Apprentice to Mentor model. We set out to increase our workforce, save time on human processes, and decrease human-to-human networks, which would allow us endless capacity and increased communication speed, which were previously staffed by human-based roles. Smith can provide value in directly realized time equivalent of hundreds of man hours. As it is trained, it evolves, and in time will take on additional duties and solve more problems.

Who should attend: PCB Designer, System Designer, Hardware Engineer, Assembly Engineer/Operator
Target audience: Beginner, Intermediate

11:00 AM – 12:00 NOON

KEYNOTE: IS PAST PROLOGUE? THE FUTURE OF THE PCB DESIGN INDUSTRY

Walden Rhines, Mentor

From Racal-Redac's initial release of a PCB and schematic software nearly 50 years, much has changed in the electronics hardware design space. Routing has become shape-based and automated. Features like component libraries, panelization, design for manufacturing and design rule checks are now the norm. Simulation and analysis tools have been developed and bolted on. And bare boards are no longer conceptualized independently, but rather considered as part of the full system.

As much as the tools have changed, so has the industry itself. Starting as offshoots of larger OEMs, then evolving to a broad mix of independent software developers – some large publicly traded entities, some tiny firms – the tool industry has of late seen consolidation. How have the technology changes influenced consolidation? And as mega-mergers such as Siemens' acquisition of Mentor Graphics take place, will the companies that make tomorrow's tools once again be parts of large, multinational conglomerates?

Perhaps no one is better positioned to chart the course of these industry changes than Wally Rhines. Rhines led Mentor for more than 24 years, making him easily the longest-tenured executive in PCB industry history. In this one-of-a-kind keynote address, Rhines will recap the PCB design industry timeline, from its unheralded early days to its current prominence. And he will lay out Siemens' strategy for Mentor, and how it will shape the industry at large.

F4: DESIGNING IN THE AGE OF PROTOTYPES

Milan Shah, Royal Circuits

We live in an increasingly connected world with new electronics products introduced every day. From coast to coast, engineers are designing everything from life-changing medical devices to new military technology to one-of-a-kind experiments for launch into space. To stay ahead of competitors, companies must be innovative and quick to market. And once a product is launched, designers must immediately start working on the next revision. PCB prototypes play a critical role in this design-revise-design product lifecycle. Prototypes are the first step in bringing new ideas. Yet, getting PCB prototypes fabricated and assembled correctly on-time and on-budget is a challenge. In this panel presentation, three CEOs from some of the industry's most respected PCB prototype manufacturing companies will discuss the challenges of PCB prototypes. Executive speakers will be Milan Shan, president of Royal Circuit Solutions; Lawrence Davis, president of Advanced Assembly, and Scott Kohno, president of Royal Flex Circuits. Drawing on nearly 45 combined years in the industry, these executives will also share practical tips, advice and resources on how to get PCB prototypes manufactured on-time and on-budget. Topics to be covered include the latest trends in PCB prototyping; growing usage of flex prototype circuit boards; common PCB fabrication and assembly mistakes; cost-saving design tips; review of different types of PCB prototyping services.

Who should attend: PCB Designer
Target audience: Beginner, Intermediate, Advanced

1:00 PM TO 2:00 PM

F5: INDUSTRY 4.0 AND IPC-2581

Hemant Shah, IPC-2581 Consortium

Listen to experts from the IPC-2581 Consortium and from IPC-Connected Factory Exchange (CFX) group about Industry 4.0 and what role IPC-2581 plays in it.

Who should attend: PCB Designer
Target audience: Beginner, Intermediate, Advanced

1:00 PM – 3:00 PM

F6: THE 10+ 21 MOST COMMON DESIGN ERRORS CAUGHT BY FABRICATION (AND HOW TO PREVENT THEM)

David Hoover, TTM Technologies

In preparation for this presentation, we talked to many of the largest PCB manufacturers in the US and abroad. We then developed a list of the most common errors found on incoming designs. We started with 10 and now, based on popular demand, we've expanded and keep updating that list! We look at each of the errors and discuss ways to find them before the designs are sent out for manufacturing. Methods we will look at include netlist comparison, design for manufacturing, and design rule analysis. We encourage attendee participation and ask folks to bring their challenges for discussion. After this seminar, the PCB designer will take back some knowledge to better assist them in using their existing tools in the market to produce better and more accurate designs.

Who should attend: PCB Designer, Fabricator Engineer/Operator
Target audience: Beginner, Intermediate

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We look at each of the errors and discuss ways to find them before the designs are sent out for manufacturing. Methods we will look at include netlist comparison, design for manufacturing, and design rule analysis. We encourage attendee participation and ask folks to bring their challenges for discussion. After this seminar, the PCB designer will take back some knowledge to better assist them in using their existing tools in the market to produce better and more accurate designs.

Who should attend: PCB Designer, Fabricator Engineer/Operator
Target audience: Beginner, Intermediate

2:00 PM – 3:00 PM

F7: EFFICIENT PCB INTERPOSER DESIGN USING A NOVEL SMART ROUTER BASED ON NEURAL NETWORKS AND GENETIC ALGORITHMS

Xiao Ming Gao, Naveid M. Rahmatullah and Taylor Hogan, Intel

As the complexity and variety of system-on-chip (SOC) and IP development increase, the platforms used to validate silicon electrical and functional performances are becoming increasingly difficult, due to time-to-market and cost constraints. To completely validate these SOC IPs, different platforms have to be designed to target different market segment requirements. Often the time to launch is critical to make sure it will not miss market opportunities. To meet these challenges, the interposers can provide flexible and low-cost solutions. It can be used to adapt silicon to a variety of platforms without changing existing designs and therefore maximize the return on investments. For example, the N-1 interposer is a special kind of PCB adapter that allows prior generation chip, the N-1 silicon to be installed on a current generation system, the N platform for validations. This facilitates platform checkout and deployment before new silicon arrival, enabling early shift left platform strategy, such as Firmware development, BIOS, and test and validation collateral developments. The design of N-1 interposer involves a few steps. First is to collect requirements and define the pin mapping between N and N-1 generation silicon. Next is to use scripts to generate netlist using this mapping file. Finally, define the board stackup and create constraints to route these connections. The last step is always labor-intensive and time-consuming because interposer board size is usually very small, and the package has more than a thousand pins, so the High Density Interconnect (HDI) design has to be used. A combination of irregular routing patterns and constraints on critical signals is beyond the capacity of the most modern automatic routing systems, and the routings have to reply on manual interactive layout. To improve the efficiency, we propose a new machine-learning-based routing algorithm. Multiple routing strategies can be run in parallel to help search the solution space of its domain. Each phase is essentially an optimization problem, and we use a Genetic Optimization engine that concurrently searches through multiple design options looking for the global best. We propose using a deep neural net as the fitness function. This neural net is trained by analyzing the features of previous successful design patterns, using hard-coded heuristics, such as crossovers, length, and congestion. Leveraging this process parallel mechanism, multi-core CPU and clusters-based computing resources can be used to evaluate multiple routing strategies at the same time. We have used the new autorouter to test both CPU and PCH N-1 interposers' layouts. The routing time is reduced from a week of manual routing to only a couple hours using the new router. The course will provide a complete interposer design flow from pin mapping, netlist generation, to final PCB component placement and routing. Focus especially on how to effectively use the proposed smart router to drastically reduce layout time and improve design quality.

Who should attend: PCB Designer, System Designer, Hardware Engineer, SI Engineer, Test Engineer
Target audience: Beginner, Intermediate, Advanced

3:00 PM – 4:00 PM

F8: OPTIMIZING HARDWARE FOR YOUR IOT SOLUTION

Sean Priddy, Creation Technologies

Most of the IoT hype is about how billions of devices will generate huge data streams that must be communicated, stored, and analyzed to provide operational visibility and insights using machine learning and AI over time and large data sets. However, often neglected is the actual hardware required to acquire sensor data, process the data, react to the data, and communicate the data over a network to other devices or the cloud. Frequently, emerging IoT solutions require the development of specialized hardware to accommodate various environmental, processing, localized storage, power, and networking requirements. Learn how to make the appropriate technical choices so your hardware is optimized for your IoT solution.

Who should attend: PCB Designer, System Designer, Hardware Engineer
Target audience: Beginner

F9: PANEL: THE FUTURE OF PCB ENGINEERS

Phil Marcoux, PPM, Moderator

A common comment from everyone involved in electronics supply chain today is the chronic "graying" of the industry, meaning a lack of younger engineers and professionals. Is this a truism? And what recruiting and management techniques are needed to attract – and keep – the millennials? Panelists include Joel Camarda, Amonix, and others.

4:00 PM – 5:00 PM

F10: 3D PRINTED ELECTRONICS: A NEW DIMENSION IN PROTOTYPING & MANUFACTURING

Simon Fried, Nano Dimension

3D printed electronics technologies are enabling developers to go from idea to working prototype in just days to enable agile electronics development and innovation. By iterating electronic circuits rapidly in-house, 3D printing will transform electronics development and manufacturing processes. During this session, delegates will learn about the disruptive and transformative effect of 3D printing on electronics design and manufacturing, specifically for the aerospace and defense sector. Understand the challenges and technological advancements needed to achieve next-gen 3D printed electronics that ensure high performance and reliability to meet aerospace and defense industry specifications and standards. Determine the scope of 3D printed electronics for a competitive business strategy, and understand how this technology is creating enhanced workflows, improved time to market and agile hardware development processes. Determine how to introduce agile electronics development processes at every prototyping stage to reduce time-to-market, increase innovation and keep proprietary design information in-house.

Who should attend: PCB Designer, Hardware Engineer, Test Engineer
Target audience: Beginner, Intermediate

F11: PANEL: UNDERSTANDING THE AS9100D STANDARD

Peter Bigelow, IMI, Moderator

Confusion appears to be growing throughout the supply chain, as it attempts to sort out just how often first article inspection needs to be performed. Manufacturers and their customers face both additional evaluations and a data avalanche, the result of the surge in acceptable quality limit (AQL) samples of FAI measurements as supplied to the customer, which then must enter, sort and distribute (as needed) all that data. It is one thing

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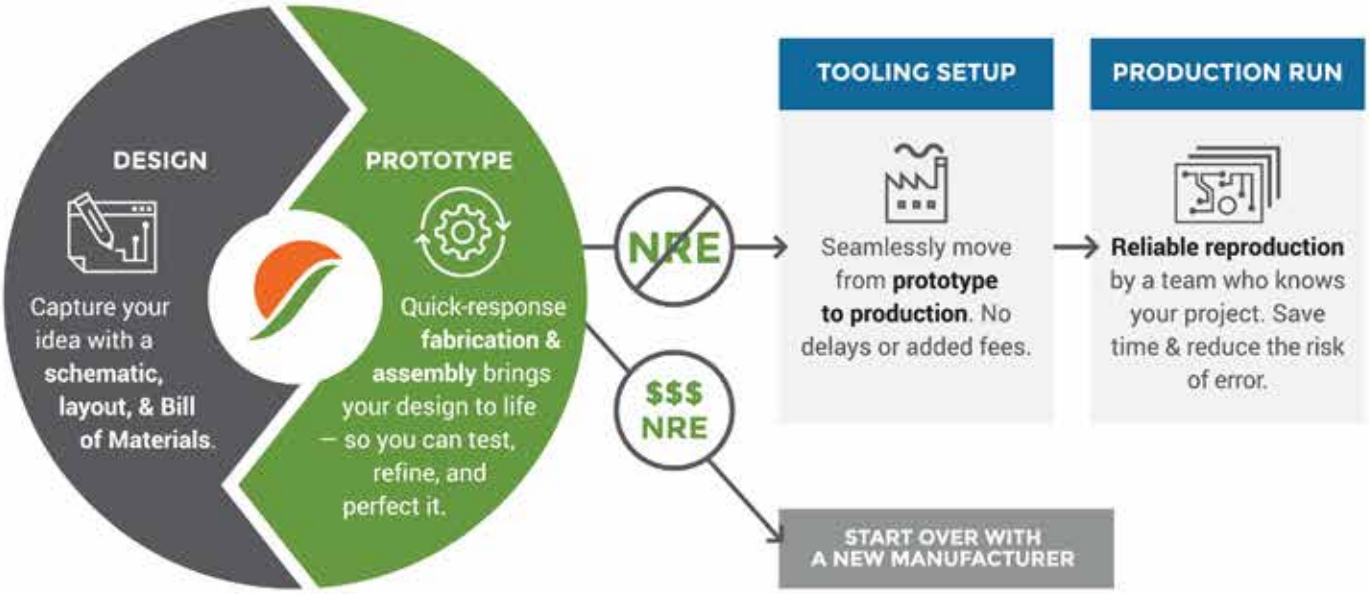

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1:00 PM – 2:00 PM

C1: ENSURE YOUR ELECTRONIC DESIGN IS RELIABLE AND ROBUST BY SIMULATION – DURING SCHEMATIC, BEFORE MANUFACTURING AND TESTING

Yizhak Bot, BQR

To verify that electronic boards are free of hidden design errors, manufacturers perform qualification and integration tests before manufacturing. If failures are detected, the manufacturer implements a root cause analysis to detect the design fault, and then turns to redesign, remanufacturing and retesting. These time-consuming efforts delay the product launch and cause the project's budget to overflow, possibly even leading to project cancellation. In this talk we will describe a new method that will detect hidden design errors by simulation in the schematic phase just before layout, manufacturing, qualification or integration tests. Using the simulator, it is possible to locate hidden design errors that may be discovered as late as during customer use. It also enables tracking of faults in existing products that already operate in the field and are used by customers. An example is a product comprising dozens of PCBs that has been operating in the field for several years, which failed suddenly. During the simulation, the cause of the failure was discovered, and the client verified it in the laboratory. Ostensibly, if the simulation had been performed on time, the problem would be entirely avoided.

Who should attend: PCB Designer, Hardware Engineer, Test Engineer
Target audience: Beginner, Intermediate, Advanced

2:00 PM – 3:00 PM

C2: RETARGETING YOUR LIBRARIES FOR NEWER, BETTER PROCESSES WITHOUT BREAKING YOUR BANK

Vince Di Lello, Cadence Design Systems

Libraries hold a company's IP, most companies will say. Libraries are built for a process that gets outdated. Manufacturing advances and newer fabrication techniques (HDI, embedded) require footprints to be built differently. This talk will show a new methodology and tools to retarget libraries for newer processes in days instead of months/years.

Who should attend: PCB Designer
Target audience: Beginner, Intermediate, Advanced

3:00 PM – 4:00 PM

C3: DESIGNING PCBS IN THE CONTEXT OF A SYSTEM

Gary Hinde, Cadence Design Systems

System design with multiple boards is a team activity for most companies. Traditional design methodologies force PCB Designers to work in silos that result in identifying system level integration issues late in the cycle or through mid-stream design reviews. There is a better way. This presentation will show a methodology that allows for managing critical high-speed system-level signals, as well as dealing with collision issues between multiple boards in an enclosure.

Who should attend: PCB Designer, System Designer
Target audience: Beginner, Intermediate, Advanced

4:00 PM – 5:00 PM

C4: MULTI-DOMAIN COLLABORATION FOR ELECTRONICS SYSTEMS DESIGN

David Wiens, Mentor

System-level product optimization requires teams across all disciplines of product development efficiently collaborate; this includes mechanical, electronics and electrical domains. This approach runs counter to the conventional "black box" design process, where teams operate largely autonomous from each other, coming together only at the end to validate the total system. Even when teams have tried to collaborate during the design process, they have been faced with tool incompatibility barriers, lack of a common review platform, and inconsistent system constraints. This session will discuss efficient methods of multi-domain collaboration, with a focus on how it enables ECAD, MCAD and cabling design teams to optimize electronics systems.

Who should attend: PCB Designer
Target audience: Intermediate

5:00 pm – 6:00 pm EXHIBIT FLOOR

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8:00 am CONFERENCE COFFEE BREAK, Sponsored by Sierra Circuits

8:30 AM – 12:00 NOON

34: DESIGN OF POWER DISTRIBUTION AND DECOUPLING

Rick Hartley, RHartley Enterprises

The power distribution section of a PCB is the foundation around which all things work in the circuit. If not designed correctly, the entire circuit is at risk from noise, to say nothing of the severely increased possibilities for EMI. Low impedance in the power bus of a digital circuit across the range of harmonic frequencies is critical. To further complicate matters, analog and digital circuits often need a much different approach for power delivery to ICs.

This course will cover the role of the major components in the power distribution network (PDN), the impact of inductance on the network, the inductance of vias, capacitors and planes, optimum location and mounting configuration for capacitors, energy delivery to IC cores and to I/O drivers, decoupling PCBs with routed power rails / PCBs with widely spaced planes / PCBs with closely spaced planes, impact of IC design on power delivery, ferrites in the PDN, analog power delivery, the real impact of ultra closely spaced planes and the huge impact of board stack-up.

Who should attend: PCB Designer, Circuit/Hardware Engineer, Signal Intgrity Engineer, System Engineer
Target audience: Intermediate, Advanced

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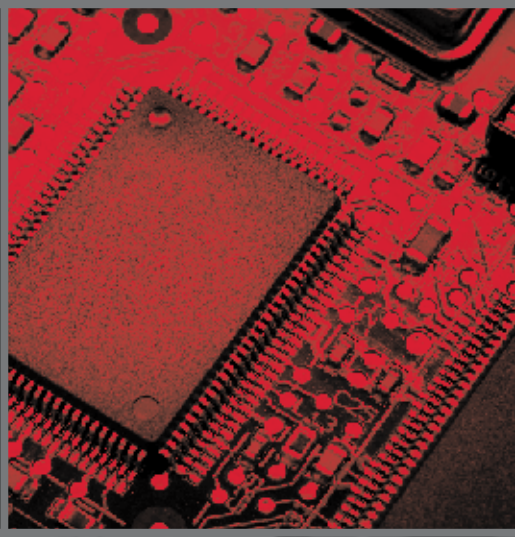

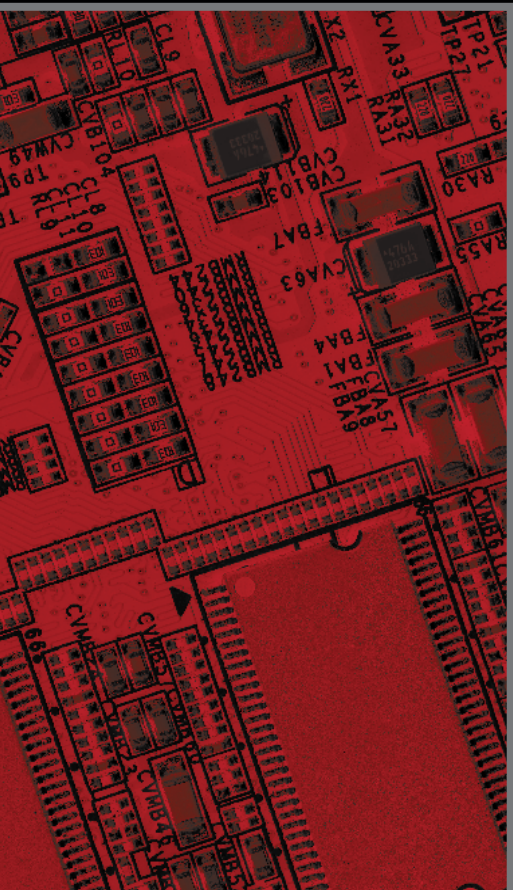

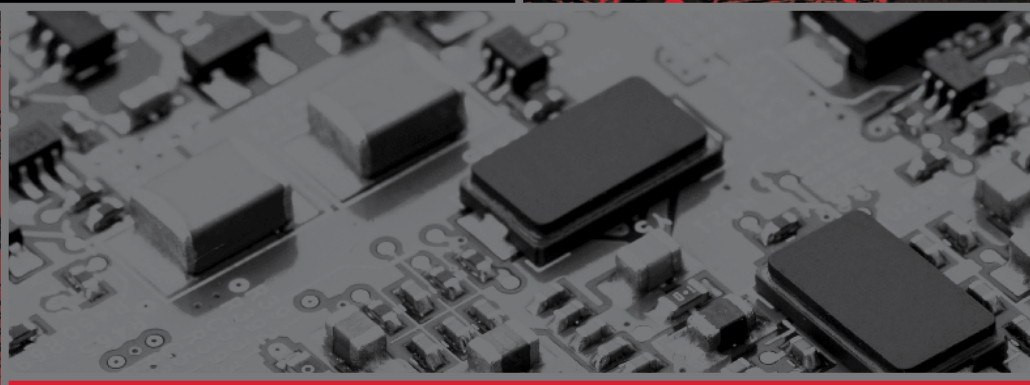

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35: PART PLACEMENT CHOICES AND CONSEQUENCES

Susy Webb, Fairfield Industries

There are many ways to place parts on any board, but clearly some ways work better for physics, electrical, and mechanical purposes. If a new board works electrically but won't interface properly with the rest of its system, it may require costly and time-consuming re-design and re-testing. Designers must understand the board, electrical and system needs, as well as typical placement and routing guidelines, and the consequences of not adhering to them. When they understand the reasoning behind these things, and the effects they have on one another, designers will intuitively know how to make good decisions for their own board designs, and so avoid problems. In this presentation, we will discuss choosing effective parts, approximate order of overall placement, placement to set up routing, board and system consequences, manufacturability, and more.

Who should attend: PCB Designer

Target audience: Beginner, Intermediate, Advanced

9:00 AM – 10:00 AM

36: INTELLIGENT DFM FOR ASSEMBLY

Kevin Webb, Mentor

Design for manufacturing (DfM) applications have been around for many years and have helped companies reduce product costs, improve quality and get products to market faster. However, PCB assembly analysis has always been difficult to align internal rules to manufacturing supplier's rules. This session discusses a new approach for implementing Assembly DfM analysis. Assembly DfM applications today must be able to intelligently evaluate the component based on many characteristics, such as JEDEC type, body and pin size, pin counts, pin types, etc., to automatically categorize itself for better and consistent DfM rule assignments. Only through an automatic assignment approach can the repeatability of analysis be achieved throughout a design process. This automatic classification approach will permit a consistent set of analyses to be performed in-house, as well as at the manufacturing facility, while considering the manufacturing processes relevant for your PCB assembly. Applications achieving this objective will serve their users better and make the benefits of assembly DfM attainable by a larger audience.

Who should attend: PCB Designer, Other

Target audience: Beginner

37: PROVIDING SOLUTIONS FOR THERMAL MANAGEMENT WITHIN RF DESIGNS

James Barry, PCB Technologies

The presentation will focus on various buildup methodologies to mitigate thermal hot spots. The basics of thermal mitigation will be presented, including heavy copper, internal and external heat sinks, material, and thermal vias. "Coin Technology" and "Air Cavity" will be discussed in depth, including how these buildups can be combined within a structure. Examples of radar boards using Air Cavity will be shown, as well as more complex buildups using a combination of coin, cavity and mixed materials. This presentation will focus on the buildup of products from a cross-sectional point of view.

Who should attend: PCB Designer, SI Engineer

Target audience: Intermediate

9:00 AM – 11:00 AM

38: THE MYSTERY OF BYPASS CAPACITORS

Keven Coates, Geospace

How do you design a high-speed digital circuit with enough bypass caps in the right area to supply all the peak power demands? You can't listen to all the expert advice because it seems they can't even agree! This presentation covers power distribution network basics and shows three approaches with simulation results for each, and some real-world experience and advice on bypassing for high-speed circuits.

Who should attend: PCB Designer, System Designer, Hardware Engineer, SI Engineer

Target audience: Beginner, Intermediate, Advanced

39: ASK THE FLEXPERTS – FLEXIBLE CIRCUIT DESIGN THROUGH TEST WITH LESSONS LEARNED

Mark Finstad, Flex Circuit Technologies, and Nick Koop, TTM Technologies

This course will cover the gamut of flexible and rigid flex circuits from two of the most recognized names in the industry; Mark Finstad (co-chair of IPC-2223) and Nick Koop (co-chair of IPC-6013). Topics covered will include mechanical design/material selection, cost drivers, bending and forming concerns, testing, and issues unique to rigid flex. Throughout the presentation, the instructors will share many real life stories of flexible circuit applications gained over 30+ years in the industry. Some of these are success stories and others not so much, but all provide excellent lessons learned. The instructors also welcome and encourage questions, and enjoy "wandering off course" with lively interactive discussions on specific topics from the class.

Who should attend: PCB Designer, Hardware Engineer, Fabricator Engineer/Operator, Assembly Engineer/Operator

Target audience: Intermediate

9:00 AM – 12:00 NOON

40: DESIGNING EMBEDDED PASSIVES AND RELATED TECHNOLOGIES

Gary Ferrari, FTG Circuits

We are faced with greater design challenges than yesteryear. Circuit densities and component counts have climbed at an alarming rate. Unfortunately, board area has not increased proportionally. Circuit speeds are increasing, requiring shorter connections and more decoupling capacitors. As a result, embedded passives – those within the printed board structure – have become more attractive. They enable reduced component count, and shorter connections. This session will provide an overview of the various embedded passives technologies.

Attendees will learn how individual embedded discrete components are manufactured, basic design principles for embedded passive devices, and concepts for planar capacitance and resistance layers.

Who should attend: PCB Designer, Electrical Engineer

Target audience: Intermediate

10:00 AM – 11:00 AM

41: DFM: GETTING IT RIGHT FROM THE START

Chris Nuttall, NCAB Group

This seminar describes how to avoid costly production problems with Gerber packages.

Who should attend: PCB Designer, System Designer, Hardware Engineer, Test Engineer

Target audience: Beginner, Intermediate

42: ARRIVING AT AN OPTIMAL STACKUP FOR PRINTED CIRCUIT BOARDS USED IN SILICON VALIDATION

Vijay Nanjai Anandan, Tessolve Semiconductor

Silicon validation of integrated circuits happens at various levels, such as the wafer, package and system levels. The PCB used for the validation at these levels has different mechanical and electrical requirements. For example, the PCB designed for volume test of ICs needs to be thick enough to remain planar when exposed to high mechanical and temperature stress, whereas PCBs designed for system level or a characterization test, apart from the above, should have better signal and power integrity. Furthermore, PCB fabrication yield has to be high, which has an impact on test hardware cost and cycle time. Arriving at an optimal stackup to meet all these requirements is a crucial part in designing the PCB required for silicon validation. Various stackup technologies used to design these PCBs include plated through-hole with backdrilling; plated through-hole with flip drilling; multi-laminate stackup with blind and buried vias; and high-density interconnect (HDI) stackup with microvias and buried vias. This presentation talks about each of these stackup technologies, their advantages and limitations when it comes to fine-pitch BGA such as 0.35mm, how it suits for a particular device type, be it digital, analog, mixed, PMIC or RF, and their fabrication processes. It aims to expose ATE/system-level test engineers and PCB designers to these stackup technologies, and show how to choose one that best suits for the application and requirements.

Who should attend: PCB Designer, Hardware Engineer, Test Engineer

Target audience: Beginner, Intermediate, Advanced

11:00 AM – 12:00 NOON

43: LEVERAGING 3-D LAYOUT TO OPTIMIZE RIGID-FLEX DESIGNS

Vern Wnek, Mentor

2-D design is no longer sufficient for today's complicated rigid-flex designs. ECAD designers need the ability to leverage 3-D layout in order to properly optimize all elements of a rigid-flex design at the product-level, with the design in its bent state within the enclosure. 3-D layout allows designers to place, route and perform design rule checks with immediate feedback regarding any potential clearance or collision issues. To truly optimize a rigid-flex design, the 3-D environment must be more than just an interpretation of 2-D information; it must provide a realistic view of how the design will be fabricated, no matter how complicated the structure. Properly leveraging 3-D layout functionality also allows the design team to left-shift mechanical validation into the PCB layout stage, making it possible to find and fix electro-mechanical design problems early to eliminate costly, late-cycle redesigns. By considering mechanical requirements during layout and ensuring efficient communication between the electrical and mechanical flows, the rigid-flex design is correctly aligned for manufacturing, avoiding last-minute changes that cost time and money.

Who should attend: PCB Designer, Other

Target audience: Beginner

44: OVERVIEW OF SEVERAL RF STRUCTURES AND HOW THEY WORK

John Coonrod, Rogers

This presentation will give an overview, in relatively simple terms, of several PCB-based RF structures and will describe the basic operations. Initially transmission line circuits will be discussed, and these types of circuits are often used to connect different RF modules together on a PCB. Expanding on transmission line circuit concepts will be discussions for couplers and filters. Finally, PCB-based antenna designs will be discussed. Basic concepts for each structure will be given, models shown, and measured results compared to model outputs. Most structures will be limited to lower microwave frequencies, but some discussion will be given for millimeter-wave frequencies.

Who should attend: PCB Designer, System Designer, Hardware Engineer, SI Engineer, Test Engineer

Target audience: Beginner

12:00 noon – 1:00 pm LUNCH-N-LEARN, Sponsored by Polar Instruments

1:00 PM – 3:00 PM

45: ELECTROMAGNETIC FIELDS FOR NORMAL FOLKS: SHOW ME THE PICTURES AND HOLD THE EQUATIONS, PLEASE!

Daniel Beeker, NXP Semiconductor

The material presented will be focused on the physics of electromagnetic energy basic principles, presented in easy to understand language with plenty of diagrams. Attendees will discover how understanding the behavior of EM fields can help to design PCBs that will be more robust and have better EMC performance. This is not rocket science, but an easy-to-understand application of PCB geometry.

Who should attend: PCB Designer, System Designer, Hardware Engineer, SI Engineer, Test Engineer

Target audience: Beginner, Intermediate

1:00 PM – 4:30 PM

46: FLEXIBLE AND RIGID-FLEX CIRCUIT DESIGN AND ASSEMBLY PROCESS PRINCIPLES

Vern Solberg, Solberg Technical Consulting

The design guidelines for flexible circuits, although similar to rigid circuits, are somewhat unique. In essence, flex circuits furnish unlimited freedom of packaging geometry, while retaining the precision density and repeatability of printed circuits. Flex circuits typically replace the common hard-wire interface between electronic assemblies. Flexible circuits, however, have significant advantages over the hard-wired alternative because they fit only one way, eliminate wire routing errors, and save up to 75% on space and weight. Because the flex circuit conductor patterns can maintain uniform electrical characteristics, they contribute to controlling noise, crosstalk, and impedance. The flex circuits will often be designed to replace complex wire harness assemblies and connectors to further improve product reliability. During the half-day tutorial program, participants will have an opportunity to review and discuss the latest revision of IPC-2223, "Sectional Design Standard for Flexible Printed Boards," which includes base material sets, alternative fabrication methodologies and SMT-on-flex assembly processes. The workshop will also furnish practical flex circuit supplier DfM recommendations for ensuring quality, reliability and manufacturing efficiency. Discussion topics: 1. Applications and use environment • Commercial/Consumer • Industrial/Automotive • Medical/Aerospace • Establishing end-use criteria. 2. Designing flexible and rigid-flex circuits • Flex circuit outline planning • Circuit routing and interconnect methodologies • Fold and bend requirements • SMT land pattern reinforcement criteria. 3. Material and SMT components • IPC standards for flex and rigid-flex dielectrics • Base material and metallization technologies • Selection criteria for SMT components • SMT land pattern development. 4. Assembly processing of flex and rigid-flex circuits • Dimensioning and tolerance criteria • Palletized layout for inline assembly processing • SMT assembly process variations and methodologies • Alternative joining methods for flexible circuits.

Who should attend: PCB Designer, System Designer, Hardware Engineer, Assembly Engineer/Operator

Target audience: Beginner, Intermediate

47: BEST DFM PRACTICES FOR BOARD ENGINEERS

Susy Webb, Fairfield Industries

There is so much more to board design than placing parts and connecting the signals electrically. Those who design the board can make a *huge* impact on the ease of fabrication and assembly just by the practices they put into place as they work. Knowledge and use of standard (best) practices, whether IPC or company standards, ensures that what is sent to the manufacturer will be understood and incorporated with minimal questions, and that can be a real time and cost savings. In this class, we will talk about good practices for building footprints, how parts might be placed for manufacturability, routing practices that are helpful, trace widths and spacings that are producible, a stackup structure that can realistically get the impedance and return needed, and documentation for the manufacturer that is complete and understandable. This presentation is not about how to build a board, but rather about the practical things the board engineer can do to help make fabrication and assembly easier and therefore increase yields and lower the cost for all.

Who should attend: PCB Designer

Target audience: Beginner, Intermediate, Advanced

48: RF AND MIXED SIGNAL BOARD DESIGN

Rick Hartley, RHartley Enterprises

This session is intended to give PCB designers an understanding of the "things" RF engineers request during PCB layout. Due to sensitivity in analog circuits, the keys to full functionality (whether designing very high-frequency analog PCBs, mixing RF with digital or mixing low-frequency analog with digital) are signal integrity and noise control in the design of the PCB.

This course will cover impedance matching and balance, signal wavelength, propagation delay, critical trace length, noise, reflections, waveguides and other RF transmission lines, ¼ wavelength couplers and filters designed into board copper, RF/Analog layout techniques and strategies, plane structures, component placement, critical routing and circuit isolation, ground plane splitting (when to and when not to), mismatched loads and other discontinuities, signal splitters, tuning transmission lines, power bus decoupling for RF vs. digital circuits and PCB stackups for mixed RF and digital circuits. (Experienced RF engineers will likely not learn anything new from this course, as the material is mainly geared for PC board designers.)

Who should attend: PCB Designer

Target audience: Beginner, Intermediate

3:00 PM – 5:00 PM

49: PCB DESIGN TECHNIQUES TO IMPROVE ESD ROBUSTNESS

Daniel Beeker, NXP Semiconductor

This presentation will give some simple definitions for ESD/EOS, and describe the important differences in the energy involved and the type of damage that can result. PCB design techniques for improving system robustness will be presented. Some new research to present and some incredible design results to share using these techniques.

Who should attend: PCB Designer, System Designer, Hardware Engineer, SI Engineer, Test Engineer

Target audience: Beginner, Intermediate

1:00 PM - 4:00 PM

50: PCB LAYOUT: PLACE AND ROUTE

Mike Creeden, San Diego PCB

With today's fast paced technology curve, everyone is learning various "islands of automation" for such topics as: DFX, material selection, high-speed-design, HDI (high density interconnect), software tool new features, signal/power analysis and many others. This class will show how islands of automation integrate into the overall flow of design, loosely referred to as place and route. Highlighting the most important aspect of the equation and that is the designer and improving design skills. Attendees will learn how and when the latest trends and technologies can be incorporated into the average CAD Layout process. They will observe solutions and real-life examples to complex challenges, learning how to improve the order of the layout process for maximum benefit. Topics covered include DfX with manufacturing collaboration to the CAD process flow; project build profile (type of circuit, end customer, environment, quantity, etc.); mechanical and 3-D; constraints, SI/PI, HDI and stackup; placement methods (if placement is poor, routing is difficult or unsolvable); routing and power management methods; verification using "correct-by-construction" methods; documentation and deliverables.

Who should attend: PCB Designers, System Designers, Circuit/ Hardware Engineers, SI Engineers

Target audience: Beginner, Intermediate

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MEHDI ABARHAM is a lead application engineer with a primary focus on electronics cooling applications. He has a doctorate in mechanical engineering from the University of Michigan. After graduation, he worked at Ford as a research engineer for two years before joining Ansys.

VIJAY ANANDAN is director for PCB engineering at Tessolve Semiconductor India. He has been with Tessolve for the past 10 years and has designed several complex test boards for top semiconductor companies for various ATE platforms and systems for digital, mixed, power management and RF applications. He has also worked with various PCB manufacturers in different regions and has thorough knowledge of PCB manufacturing. He has a bachelor's in electrical and electronics engineering from Anna University, Chennai, India.

CRAIG ARMENTI is a PCB marketing engineer for Mentor Graphics with a focus on the Xpedition tool suite. Over the past 25 years he has held marketing and application engineering positions with several major telecommunication and software companies. He holds a bachelor's in electrical engineering technology and an MBA in management. Prior to joining Mentor, he worked in PCB design, hardware management and application engineering at Blackberry, Foxconn, RadiSys and Nortel.

JAMES BARRY is has over 40 years in manufacturing, design, engineering and reliability experience. His background is completely in PCB technology, including assembly. He is trained in engineering, applications, materials and failure analysis. He has held various positions within the PCB industry, ranging from manufacturing, R&D, sales and marketing, engineering, and corporate and executive levels. Currently he is sales and marketing manager for PCB Technologies of Israel.

BILL CARDOSO, PH.D., started Creative Electron in his garage after 10 years with Fermilab. Creative Electron is now the largest US manufacturer of x-ray systems to the electronics industry. At Creative Electron, he leads the team of engineers that designs and manufactures x-ray systems. He received his associate's degree at 13 and went on to achieve a bachelor's, master's, and Ph.D. in electrical and computer engineering. He also has an MBA from the University of Chicago. Cardoso sits on the technical committees of SMTAI, SMTA Counterfeit Conference, SMTA LED Conference, Components for Military and Space Electronics Conference, SPIE Photonics, and the IEEE Nuclear Science Symposium. He has written two books and over 150 technical publications. He started his first company at 17 in Brazil, selling it a few years later to work for the Fermi National Accelerator Laboratory (Fermilab).

With more than 40 years of experience in electronic system design and EMC, **DANIEL BEEKER** provides applications support for NXP Automotive customers worldwide. He also supports NXP customers globally with special function development tools and instrumentation (almost all of the "LFxxx" tools on the NXP website). He also specializes in EMC and signal integrity design techniques for systems and PCBs, especially in low layer count designs. Beeker teaches field-based design techniques at NXP and industry conferences worldwide. Beeker is also involved with NXP IC package design and IC development tool teams to support improved EMC performance.

PETER BIGELOW is president and CEO of IMI Inc., a Haverhill, MA-based PCB fabricator. He has over 35 years' experience in sales, marketing, planning, operations and general management with large and small manufacturing companies including Burndy Connectors, International Paper, Rostra Holding, and Beaver Brook Circuits, where he was president and CEO. He currently serves on the board of directors of Record Journal Publishing, and previously has served on the board of Brookfield Engineering Laboratory, where he was also acting COO, and on the IPC board of directors. He is a longtime columnist for PCD&F/CIRCUITS ASSEMBLY.

YIZHAK BOT has more than 25 years of experience in reliability and safety engineering for large projects, including electronic circuits and mechanical components for defense, aerospace, telecom, manufacturing, medical, etc. He was the program manager of many defense and commercial projects of more than $25 billion. He has written articles for leading magazines, conducts seminars and gives lectures worldwide. He is also the inventor of CARE, fiXtress and apmOptimizer technology, which help designers develop more robust products. Since 1989, he has been president and CTO of BQR, a professional testing and simulation service provider and software developing firm for the EDA market. Bot is a Certified Reliability Engineer from American Society for Quality Control (ASQC) and has a degree in electronic engineering from Tel-Aviv University.

RALF BRUENING is product manager and senior consultant at the Zuken EMC Technology Centre in Paderborn, Germany. He holds a degree in computer science, electrical engineering and economics from the University of Paderborn. He has 30 years of experience in electronics and EDA. He has longtime technical co-responsibility for Zuken's high-speed design, signal integrity, power integrity and EMI solutions. Part of his responsibility is to help customers with practical signal- and power-Integrity problems and in enhancing and optimizing their PCB design flow. He is an active member of the IBIS Open Forum and regular speaker at national and international conferences.

CHRIS CARLSON came to Altium in August 2007 and has a background in power electronics, data acquisition, and controls. Carlson earned his bachelor's degree from Oregon State University in 1993 and has worked as a design engineer in the bio-medical, industrial controls, motor drive, and defense industries. Carlson has developed multiple multi-board products and has been the cognoscente engineer on several system-level projects.

KEVEN COATES has been a development engineer at Geospace Technologies for five years, where he works designing low-noise seismic recording devices, industrial battery testers/chargers, and battery protection circuits. His work concentrates on embedded processors, low-noise circuits, medium-power circuits, battery safety, and battery management. He spent the previous 20 years working for Texas Instruments specializing in high-speed PCB layout/signal integrity, BGA layout, thermal issues, and PCB-friendly BGA packaging for consumer and automotive applications. He holds a bachelor's degree from Texas A&M University.

JOHN COONROD is technical marketing manager for Rogers Corp, Advanced Connectivity Solutions division. He has 30 years of experience in the PCB industry. About half of this time was spent in the flexible PCB industry on circuit design, applications, processing and materials engineering. The past 16 years have been spent supporting high-frequency circuit materials involving circuit fabrication, providing application support and conducting electrical characterization studies. He is chair for the IPC-D24C High Frequency Test Methods Task Group and holds a bachelor's in electrical engineering from Arizona State University.

PAUL COOKE has more than 30 years of experience in printed board (PWB) design and manufacturing. He has held senior positions in operations, quality, process engineering and field application

engineering at some of the top North American PCB manufacturers. He has served on a number of IPC technical committees for standards development, and recently received an award for contribution to IPC-9121, "Troubleshooting for Printed Circuit Boards." He has coauthored numerous technical papers, and works with Tier 1 companies, focusing on PCB design and reliability. He has provided DfM consulting services to the industry, along with extensive training/educational presentations from PCB 101 through enhanced reliability. His current position is focused solely on working with designers in the avionics and space industry to design and develop products with extended life and long-term reliability in harsh environments.

MICHAEL CREEDEN has over 40 years of industry experience as a PCB designer, applications engineer and business owner. He is an IPC Designer Certification Master Instructor CID+, and was a primary contributor for the CID+ (IPC-CID+ Advanced Certified Interconnect Designer) curriculum. He teaches IPC-CID/CID+ curriculum through EPTAC, and is a community college instructor. He owns San Diego PCB, which employs 20 designers, utilizing most of the major CAD tools.

LAWRENCE DAVIS is president of Advanced Assembly.

JIM DELAP is an electronics product manager for Ansys, working with the company's customers and research team to provide the highest quality simulation workflow. He has a master's in electrical engineering from the University of Virginia, and has been working in the microwave and signal integrity field for over 20 years. He has designed products ranging in frequency from DC to mm-wave, and has several published trade journal and conference articles. His current interests include helping customers solve challenging electro-thermal problems.

VINCENT DI LELLO, CID+, has designed PCBs ranging from the Pebble Watch to boards that have gone into space and inside Las Vegas machines. A product engineer, he makes designers' lives easier by influencing Cadence software development.

A cofounder of Nano Dimension, **SIMON FRIED** leads its USA activities, overseeing business development, marketing, sales and product management for this revolutionary additive technology. With experience working in the US, Israel and throughout Europe, he has held senior and advisory roles in startups in the solar power, medical device and marketing sectors. Previously, he worked as consultant on projects covering sales, marketing and strategy across the automotive, financial, retail, FMCG, pharmaceutical and telecom industries. He also worked at Oxford University researching investor and consumer risk and decision-making.

GARY FERRARI is director of technical support, Firan Technology Group. He has more than 35 years' experience in electronics packaging and has held senior operations, quality and engineering positions, most recently as executive director and cofounder of the IPC Designers Council. He chaired the IPC Technical Activities Executive Committee, provided DfM consulting services, and spearheaded IPC's PWB Designer Certification Program. He was inducted into the IPC Hall of Fame in 2015.

RAY FUGITT has more than 30 years of printed circuit board experience. He spent 15 years in manufacturing, 11 with Hadco. Joining Advanced CAM Technologies as an application engineer, he supported the CAM350 product through PADS and later the Innoveda mergers. In 2002, he joined Downstream Technologies in technical marketing and later technical sales positions. He continues to support and train for both the BluePrint PCB and CAM350 products.

MARK FINSTAD is senior application engineer for Flexible Circuit Technologies. He has over 30 years of experience designing and manufacturing flexible circuits for commercial, medical, and military/avionics applications. He co-chairs the IPC-2223 Design Standard for Flexible Printed boards and coauthors the Ask the Flexperts column for *PCD&F* magazine. Finstad is also a regular columnist for several other industry publications.

XIAO MING GAO, PH.D., has been working at Intel for 20 years and has extensive experience in signal and system, I/O circuit design, signal and power integrity analysis, and high-speed platform design. He holds bachelor's, master's and Ph.D. degrees in electrical engineering. He has four patents and other pending applications.

JIM HALL is principal consultant and resident Lean Six Sigma Master Black Belt with ITM Consulting. His area of responsibility includes working with OEMs, contract assemblers, and equipment manufacturers to solve design and assembly problems, optimize facility operations, as well as teach basic and new technologies in private and public forums throughout the worldwide industry. Since joining ITM in 2000, he has helped clients in such areas as SMT implementation and assembly facility setup, manufacturing yield improvement, and process audits and improvement. He is coauthor of the SMTA Process Certification Course.

ROBERT HANSON, MSEE, has more than 40 years' experience in design, manufacturing and testing. He has bachelor's degrees in industrial engineering and business administration and a master's in electrical engineering. Hanson has been a digital design engineer at Boeing, Rockwell, Honeywell, and Loral. He teaches and consults internationally to corporations, conventions, universities, and other entities.

With 20 years of experience dealing with PCB signal integrity, **BILL HARGIN** served as product manager for Mentor Graphics' HyperLynx SI software. He currently serves as director of North American marketing for Nan Ya Plastic's PCB laminate division. More than 10,000 engineers and PCB designers worldwide have taken Hargin's workshops on high-speed PCB design, and he has spent much of the past five years focused on stackup design and PCB materials selection.

RICK HARTLEY is principal of RHartley Enterprises, resolving noise, signal integrity and EMI problems. Hartley has a degree in engineering from Ohio Technical Institute and 49 years of experience with companies such as L3 Avionics and BF Goodrich. He is a past member of the Editorial Review Board of *Printed Circuit Design* magazine and has written numerous technical papers and articles on methods to control noise, EMI and signal integrity.

GARY HINDE has been involved in PCB design since his apprenticeship started in 1975. While at Schlumberger Instruments he was involved in design and layout for a diverse range of products such as laboratory instrumentation (digital voltmeters, frequency response analysers, remote data logging and industrial transducers), aircraft flight control simulators, ground warfare simulation systems and security access systems. In 1991, he joined Cadence Design Systems as an application engineer, providing support for internal teams and customers. He has worked with a number of companies worldwide and

is currently helping to develop electronic hardware system solutions for multi-fabric designs.

TAYLOR HOGAN has been working in electronic design automation for over 30 years. His research interests include genetic optimization, machine learning, and functional programming. He holds a bachelor's in computer science and a master's in electrical engineering. He holds several patents in the area of constraint-driven optimization of multi-substrate designs.

JEREMY HONG comes from a very hands-on and pragmatic hardware design background. He has dealt with complex mixed signal circuit board design and layout (40+ layer PCBs). Now he is a hardware reverse-engineer for Caesar Creek Software, but still does design work through a company he started in high school, Hong's Electronics. He lives in Dayton, Ohio.

DAVE HOOVER is a senior field application engineer at TTM Technologies, where he supports some of its top telecom customers. He has 40+ years' experience in PCB fabrication, and has been involved with the development of HDI, microvias and other leading high-speed technologies. His career includes PCB fabricators such as Hadco/Sanmina, Data Circuits, Litronic Industries, and Multek.

SCOTT KOHNO is president of Royal Flex Circuits.

NICK KOOP is a senior field application engineer for TTM Technologies and has over 30 years of design, manufacturing and management experience in the flexible circuit industry. He developed and applied advanced PCB technologies to support a wide range medical, military, and global security applications. He is vice chairman of the IPC Flexible Circuits Committee, co-chair for the IPC-6013 Qualification and Performance Specification for Flexible Printed Boards Subcommittee, and coauthors the *Ask the Flexperts* column for *PCD&F* magazine.

RICHARD LEGASPINO is currently a senior PCB engineer at Analog Devices Inc. He graduated in 1994 from Cebu Institute of Technology, Cebu City with a bachelor's degree in electronic and communications engineering. He has three years' experience in hardware engineering at Acer Inc. Taiwan and five years' experience as test engineer at Teradyne Philippines LTD, Cebu. He joined Analog Devices Philippines on May, 16 2006 as test manufacturing engineer. He currently leads the simulation team at Analog Devices Philippines that supports signal and power integrity simulation requests across ADI sites.

MARK LAING has over 25 years' experience in PCB manufacturing, with particular strengths in test and inspection methodologies with three test companies: Marconi instruments, GenRad and Teradyne. He then moved into software solutions for Router Solutions. Since 2010, he has worked for Mentor's Valor division as a product marketing manager and business development manager. He has a bachelor's in electrical and electronic engineering from Loughborough University (UK). He has been granted two patents, one in the UK and one in the US, and recently filed a third one.

DENNIS NAGLE has been involved with high-speed PCB design for over 29 years. At Cadence Design Systems, he is a product engineering architect, responsible for driving the technical roadmap for the Allegro Sigrity SI product line and the High-Speed Constraint Driven Flow. Prior to that, he held technical marketing and applications roles in various capacities for Cadence's PCB design products. Before joining Cadence, he worked at Data General. He has a bachelor's in electrical engineering from Worcester Polytechnic Institute.

CHRIS NUTTAL joined NCAB in 2009 as UK operations director. In 2010, he became NCAB's quality and technical manager for the worldwide group. Prior to NCAB, he was quality manager and later supply chain director of the UK's largest independent PCB operation, with partners in China, Taiwan, Korea, Malaysia, India and UK. His responsibilities included purchasing, sourcing, logistics and warehousing. Previous to that, he was a quality engineer for tier 1/tier 2 automotive customers at a PCB manufacturer in Scotland. He has a master's in quality management.

SEAN PRIDDY has a 20+ year diverse background in embedded electronics product development across consumer electronics, industrial, and DoD markets. As a senior design engineer, he has developed many wireless communications products spanning cellular, Bluetooth, 802.15.4, and other proprietary networking technologies. As a systems architect, he has created a software reconfigurable wireless sensor gateway and cloud-based management platform for IoT solutions. Now as the business development director for Creation Technologies, he provides guidance to customers developing novel IoT hardware solutions.

STEVEN G. PYTEL JR. is principal electronics product manager at Ansys. He has a Ph.D. in signal integrity from the University of South Carolina. He previously worked at Intel as a signal integrity and hardware design engineer where he helped design blade, telecom, and enterprise servers. He has over 50 publications, with an invited book chapter on signal integrity simulation within Maxwell's Equations: *The Foundations of Signal Integrity,* authored by Paul Huray. His current research interests focus on electro-thermal design challenges for digital and high power electronic devices.

NAVEID M. RAHMATULLAH has been working for Intel for 18 years, managing multiple hardware platform teams. He has been leading the board design process and methodologies within Intel to maximize efficiency and deliver high quality platforms for client, server, and IoT products and IP validations. He holds a bachelor's in electrical engineering, and has authored several technical papers.

WALDEN RHINES is president and chief executive of Mentor, a Siemens business. He was previously CEO of Mentor Graphics for 23 years and chairman for 17 years. Prior to joining Mentor, Rhines was executive vice president of Texas Instruments' Semiconductor Group. During his 21 years at TI, he was president of the Data Systems Group and held numerous other semiconductor executive management positions. He has a bachelor's in engineering from the University of Michigan, a master's and Ph.D. in materials science and engineering from Stanford, and an MBA from Southern Methodist University.

ALEXEY SABUNIN joined Altium in 2013 and has extensive experience in the electronics design industry. He earned his Master's degree in Electronics Design from Vladimir State University in 2004 and has worked as PCB layout engineer in the Aerospace industry. In 2006, he worked on the support team for an Altium reseller, and eventually joined Altium in 2013 as a Product Manager. Since the early days of his professional career, Alexey has participated in various research and development projects for EDA tools. In recent years, Alexey led research initiatives that contributed to the development and implementation of many key features in Altium Designer, including Draftsman and Multi-Board design.

HEMANT SHAH has been with Cadence Design Systems, SPB division since 2000, most recently as product management group director – Allegro PCB & FPGA products. Previously, he was engineering director for advanced development at Xynetix Design Systems, where he also held a product marketing director role. He holds a bachelor's in electrical engineering and a master's in computer science.

JAY SHAH is lead application engineer at Cadence Design Systems. He predominantly works with signal integrity/power integrity tools, as well as PCB design tools with customers such as Intel, TI, ARM, Broadcom and Google. He helps customers in software evaluation and debugging issues. Prior to Cadence, he was involved with hardware design, simulation and testing with eInfochips.

MILAN SHAH is president of Royal Circuit Solutions, which he purchased in 2008. He began his technology career at Apple Computer. From there he moved to Sony as director of multimedia technologies and introduced leading-edge technologies to the North American markets. He has a bachelor's in computer information systems and business communications from Western Michigan University, and also an MBA.

VERN SOLBERG holds several patents for IC packaging innovations, including the folded-flex 3D package technology and is the author of *Design Guidelines for Surface Mount and Fine-Pitch Technology*. He is a speaker and instructor supporting several industry organization technical programs, including IPC and SMTA. He is currently an IPC Ambassador Council member, chairman of the task group that developed the IPC-7094, "Design and Assembly Process Implementation for Flip Chip and Die Size Components," and a certified IPC trainer for IPC-A-600, "Acceptability of Printed Boards."

KEN TAYLOR never designed a board in his life, nor did he build one, and he's too old to begin now. He began his career teaching high school and college, then returned to college, eventually becoming a physicist with a global chemical corporation before moving to exciting stuff like rocket propulsion and submarine acoustics. Next came 25 years of international sales and marketing with Tektronix before moving to Polar Instruments in 2001 to manage Polar's US operations. Notwithstanding, he understands the physics of PCB transmission line impedance and has worked with engineers, board designers and board manufacturers during his entire Polar career. His teaching experience helps him convey concepts in the least threatening way.

KEVIN WEBB is a technical marketing engineer for the Valor Division of Mentor, with in-depth knowledge of Valor NPI, automation and PCB manufacturing processes.

SUSY WEBB, CID, is a senior PCB designer with 37 years of experience. Her career includes experience in coastal and oceanographic oil exploration and monitoring equipment, point-to-point microwave network systems, and CPCI and ATX computer motherboards. She is a regular speaker at PCB, IPC and international design conferences and consults for individual companies and Designers Council chapters. Her presentations discuss practical implementation of complex engineering concepts into board layout, and methods to improve the overall design and flow of printed circuit boards. She has set up company standards, documentation, procedures, and library conventions for several companies. She a former writer/columnist for *PCD&F* magazine, and a judge for Mentor's Technology Leadership Awards. Webb is also an active member of the IPC Designers Council Executive Board and education committees.

DAVID WIENS joined Mentor in 1999 through the acquisition of VeriBest. Over the past 30+ years, he has held various engineering, marketing and management positions within the EDA industry. His focus areas have included advanced packaging, high-speed design, routing technology and integrated systems design. He holds a bachelor's in computer science from the University of Kansas.

VERN WNEK is a Technical Marketing Engineer for the Xpedition software group. A PCB designer by trade in this great industry for 38+ years. Coming full circle to work for Mentor Graphics, a Siemens Business, after designing boards, working in board houses, assembly houses and test facilities. He has worked for service bureaus and some of the largest companies in the world, military to commercial. And now, Mentor Graphics a Siemens Business, after using the tools for over 20 years. Xpedition has been the source of his livelihood since the days of Veribest. Seeing new versions come and go, and stood side by side with designers as Mentor Graphics became the leader in PCB design software worldwide. Throughout the years, and the different PCB design tools, he states that he has ended up with the best of the best.

ALBERT YANEZ is executive vice president and president of the Americas of AsteelFlash Group. He served as general manager and executive vice president of WW operations at Serious Energy, where he was instrumental in building a leading company in green building materials. He has over 25 years of international business, operations, equipment engineering and manufacturing engineering experience. He has held several positions such as corporate director of program management for Monierlifetile (LaFarge). He also served as general manager of Southwall Technologies, and was on the core management team of Manufacturers Services Inc., where he streamlined operations for Hewlett Packard's laser jet and plotter manufacturing divisions. He also held senior management positions at Western Digital. He was part of the team that founded Trimedia, which became Hitachi Metals Trimedia.

PHIL ZARROW founded ITM Consulting in 1993, and has been involved with PCB fabrication and assembly for more than 35 years. His expertise includes the manufacture of equipment for PCB fabrication and assembly of through-hole and surface mount technologies. In addition to his background in automated assembly and cleaning, Zarrow is recognized for his expertise in SMT soldering and design and implementation of SMT placement equipment and reflow soldering systems. Having held key technical and management positions with Vitronics, Excellon-Micronetics and Universal Instruments, he has extensive hands-on experience with setup and troubleshooting through-hole and SMT processes throughout the world. During his tenure as director of technology development for GSS/Array Technology, he was responsible for specifying and setting up medium- and high-speed assembly lines, as well as investigating and implementing emerging and leading-edge technologies, equipment and processes. He is coauthor of the SMTA Process Certification Course.

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